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Trustworthy Systems Group

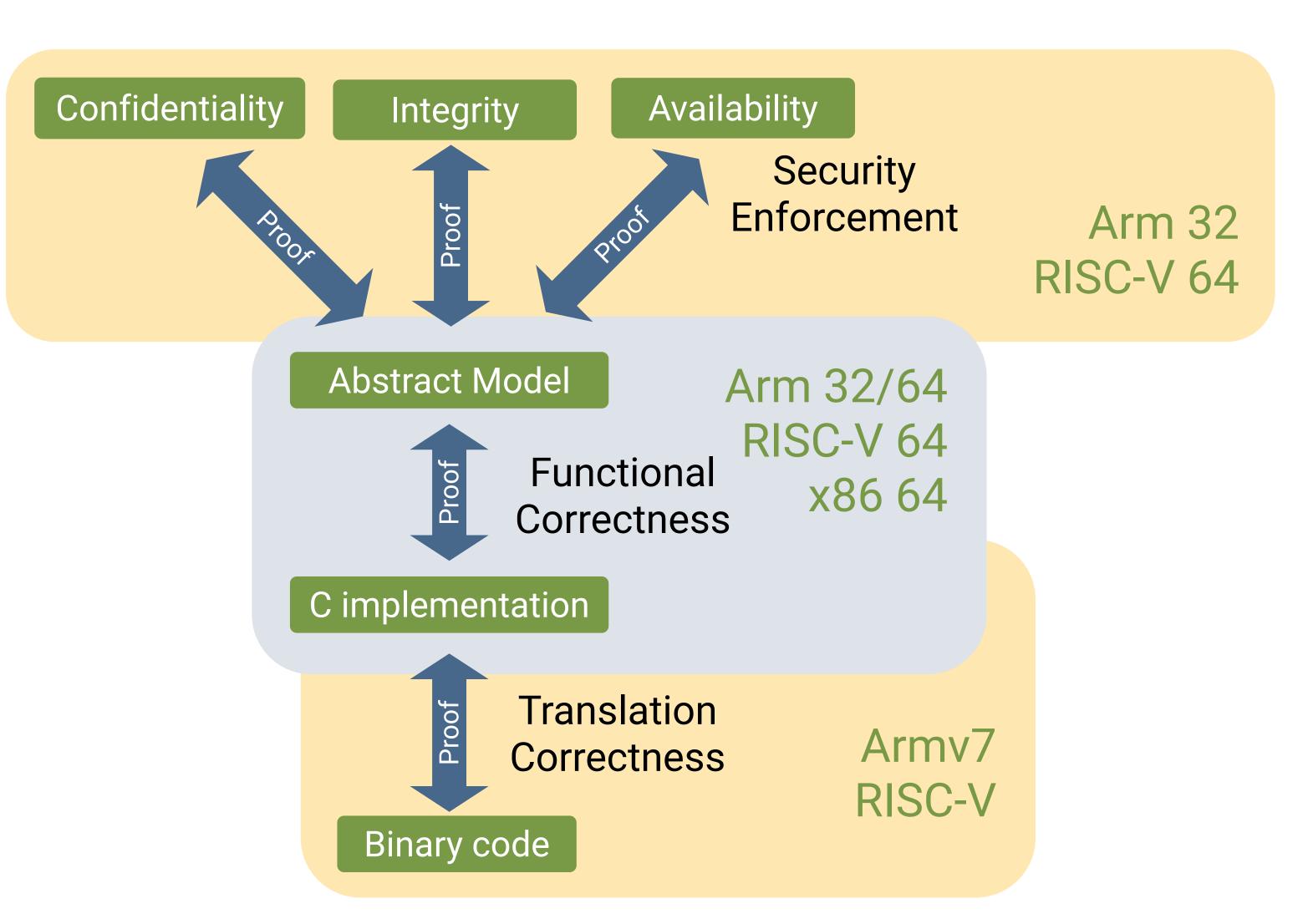
Verification Status of Time Protection and Microkit-based OS Services

Dr Rob Sison

Senior Research Associate, UNSW Sydney r.sison@unsw.edu.au



sel4 The verified seL4 OS microkernel



Verification Status of Time Protection and Microkit-based OS Services, Oct'24

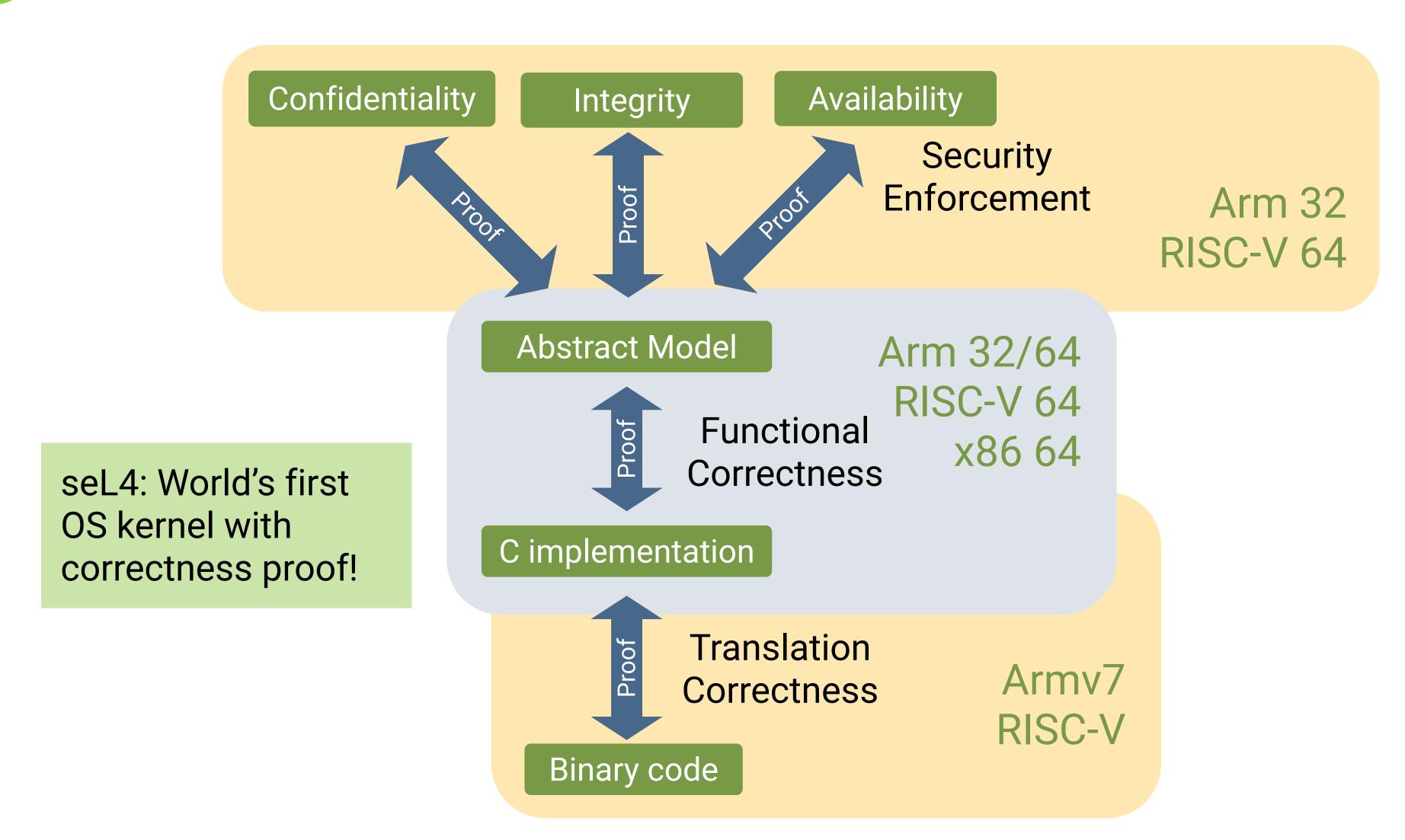


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seld The verified seL4 OS microkernel



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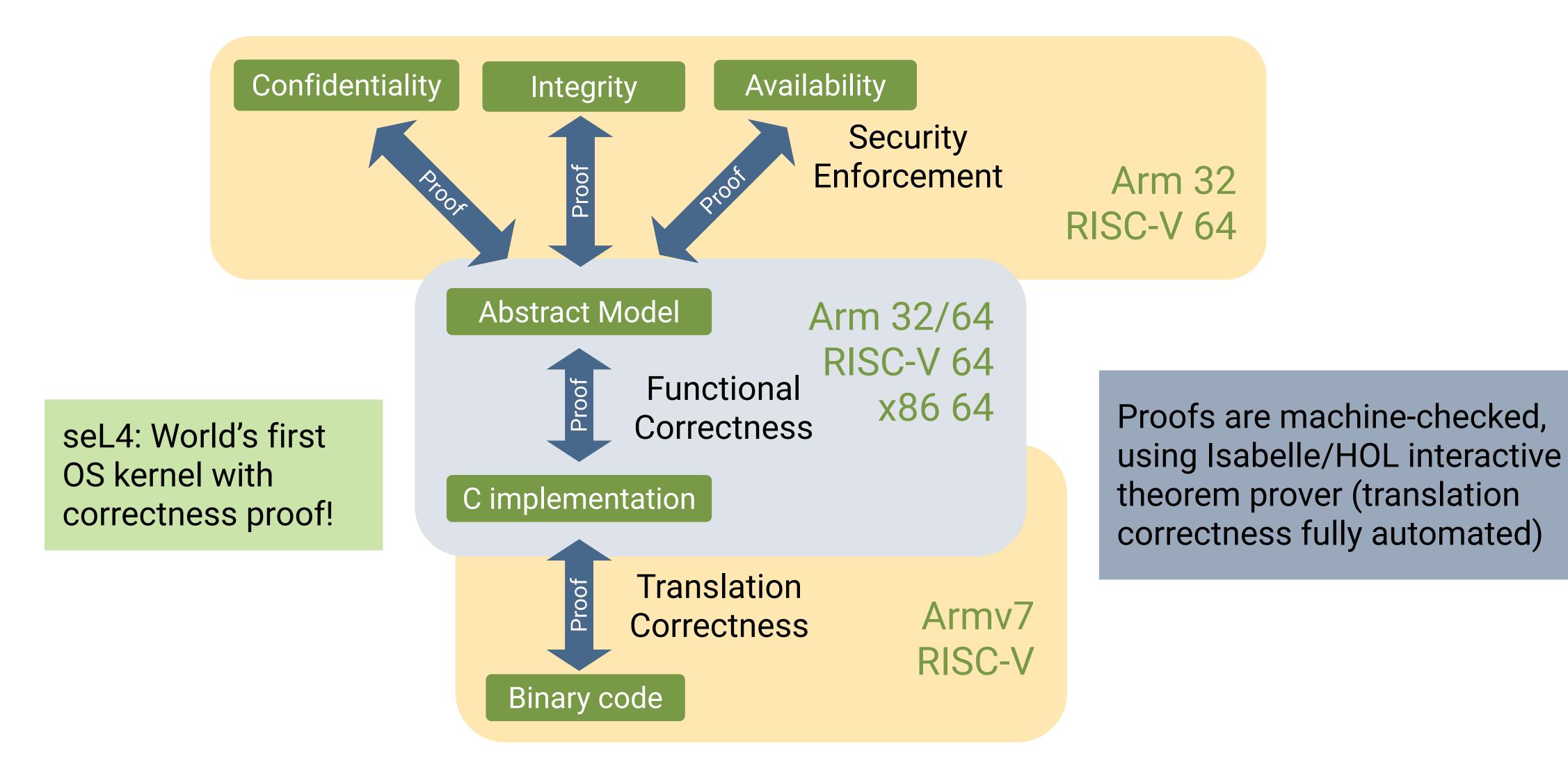


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Seld The verified seL4 OS microkernel



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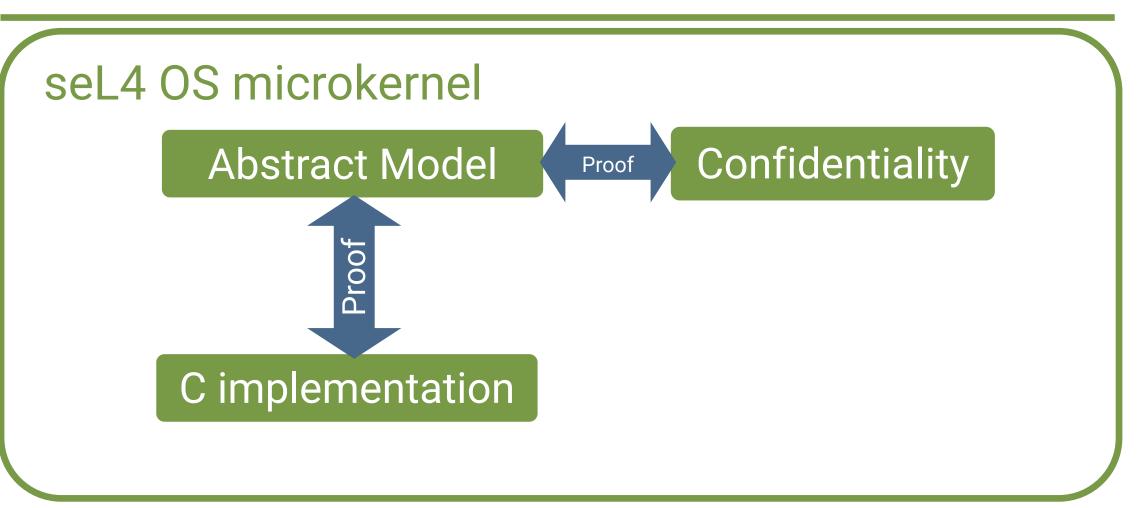


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syscall interface

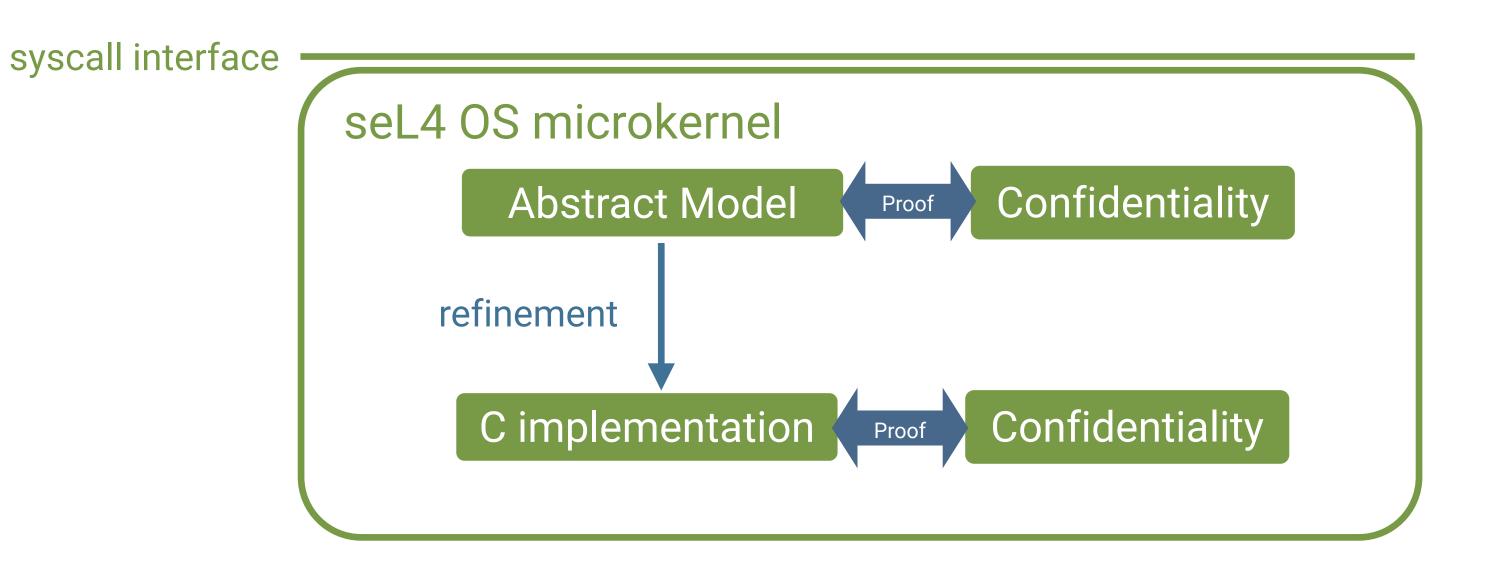


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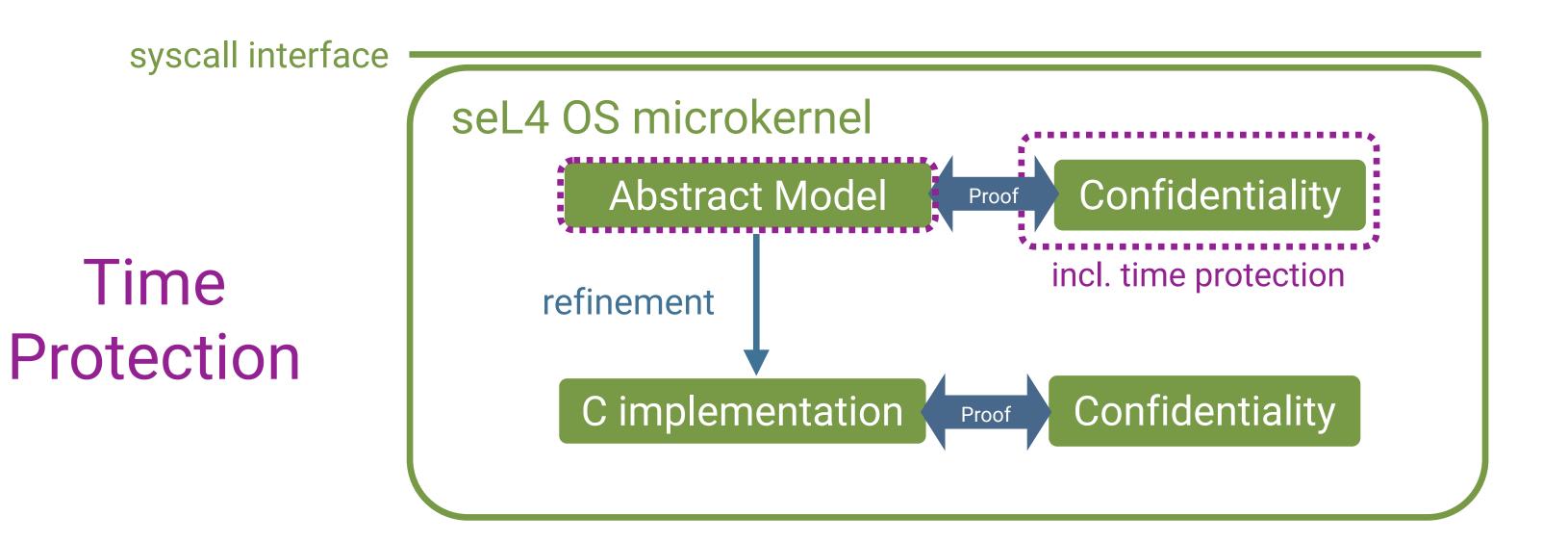




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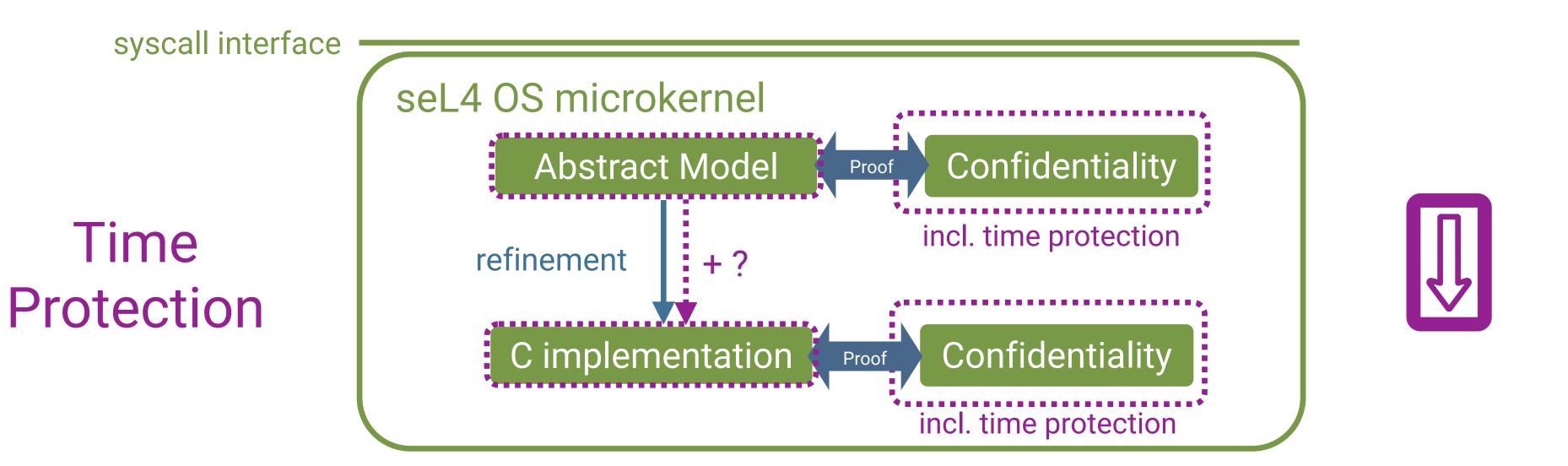










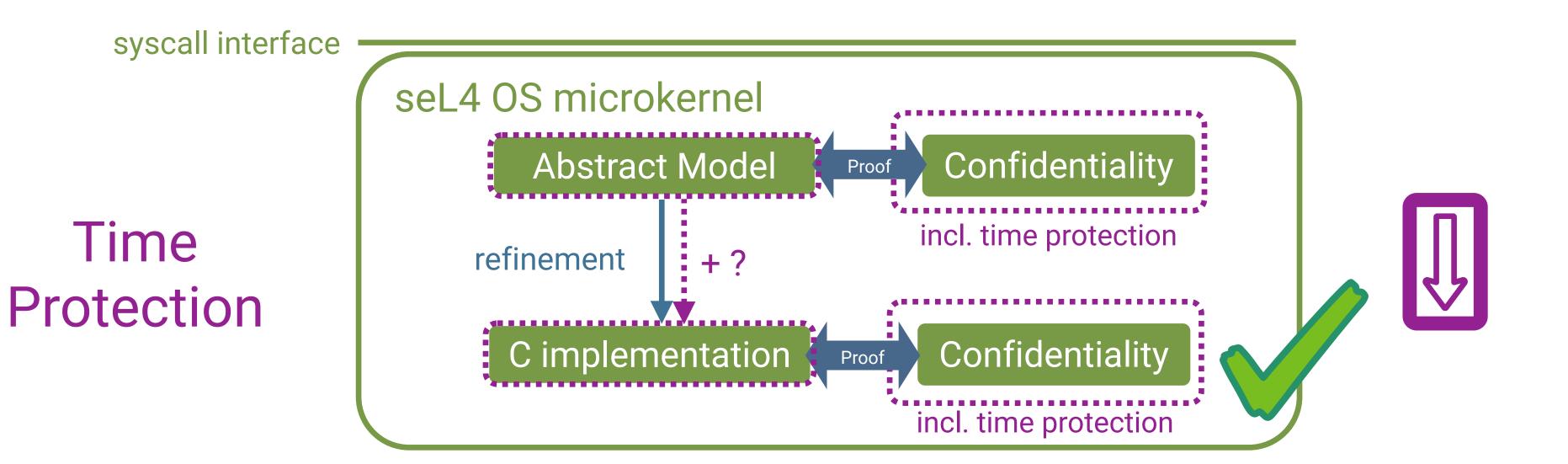




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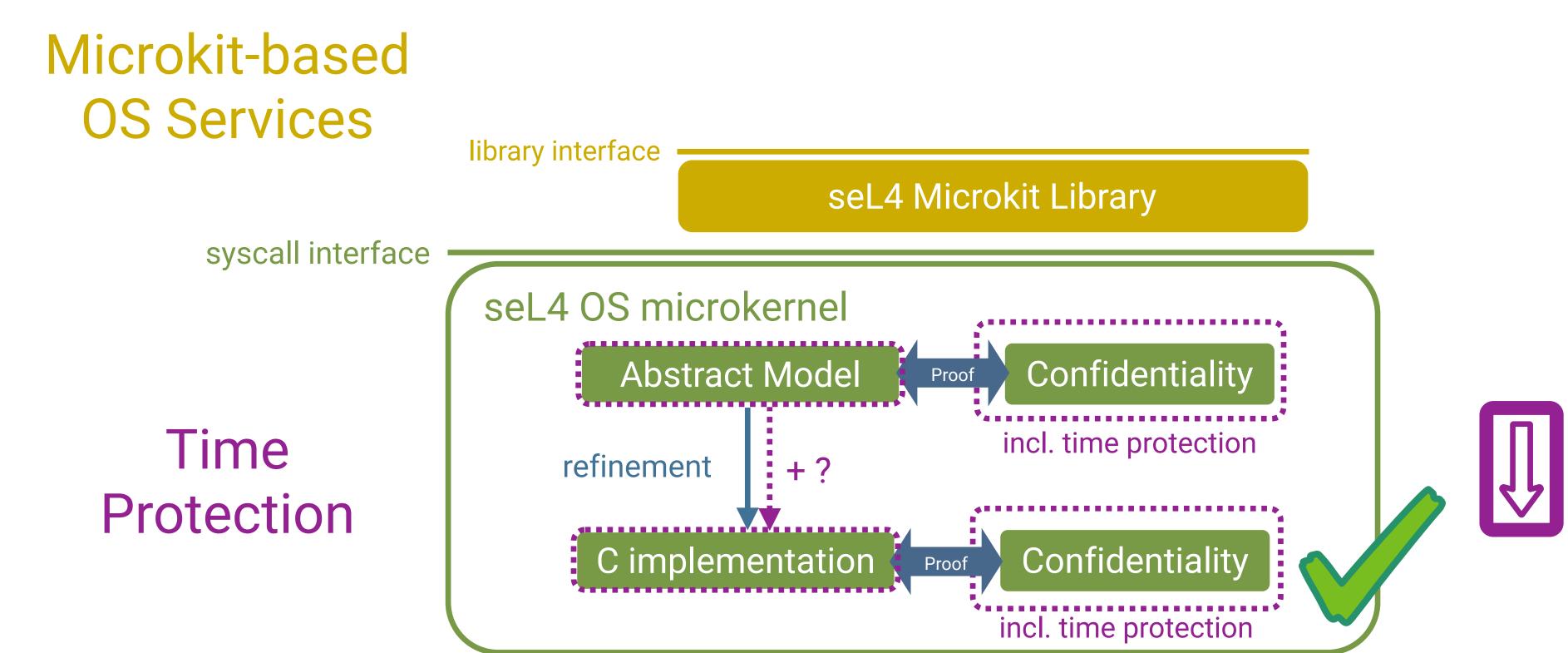




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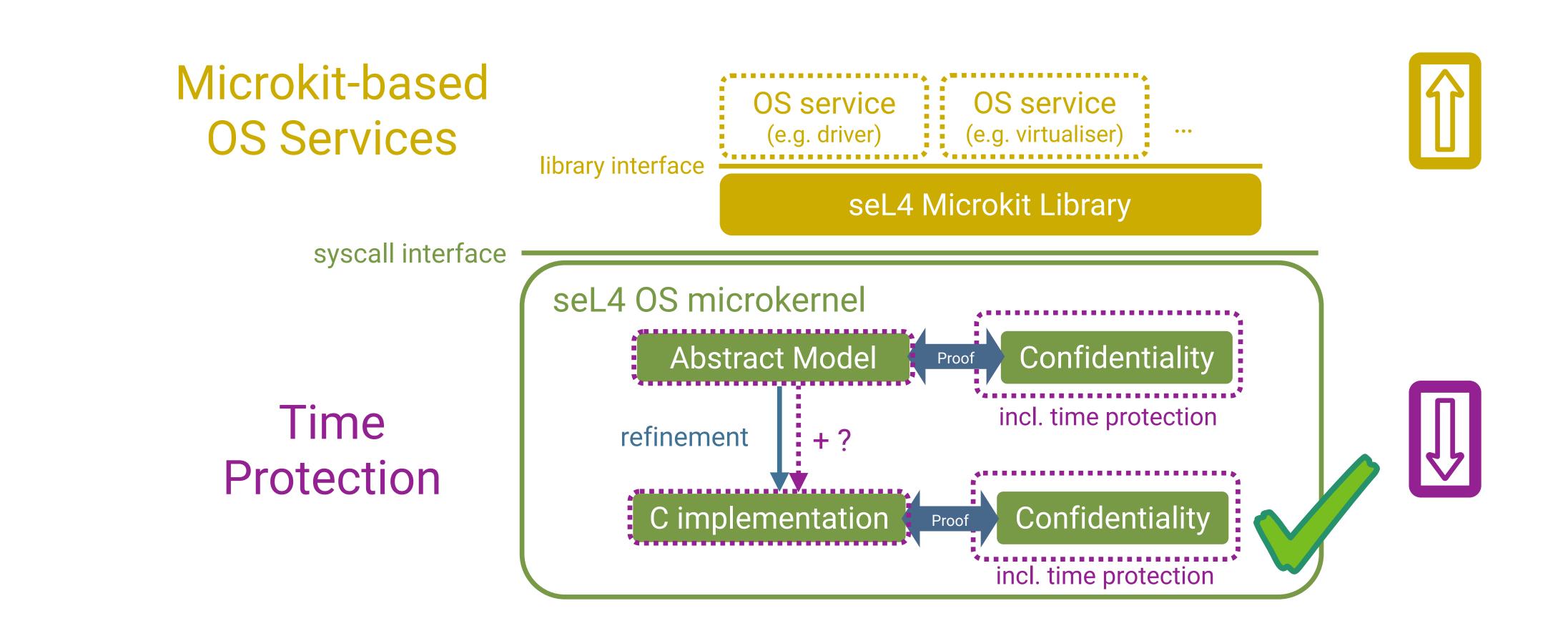








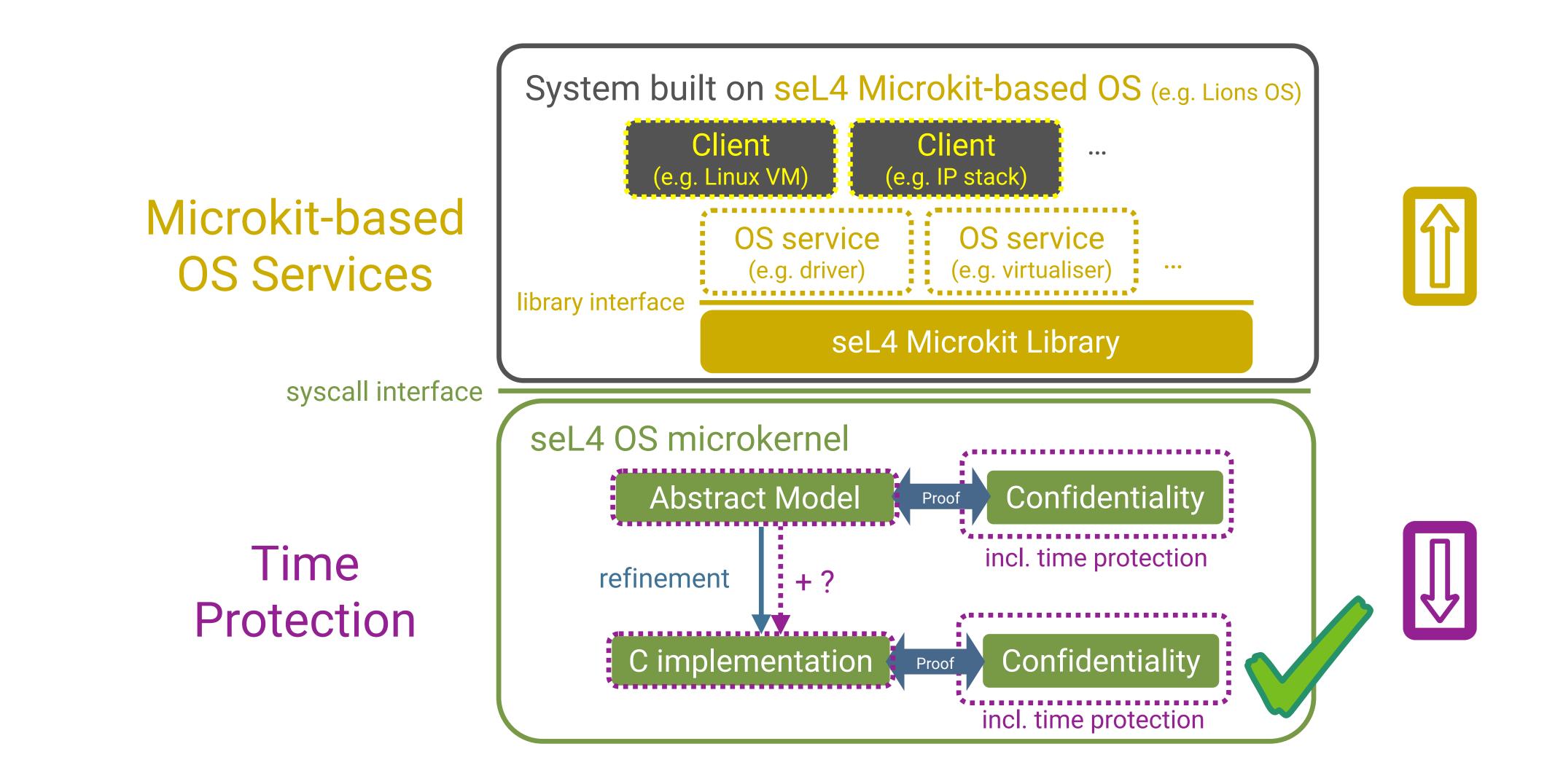




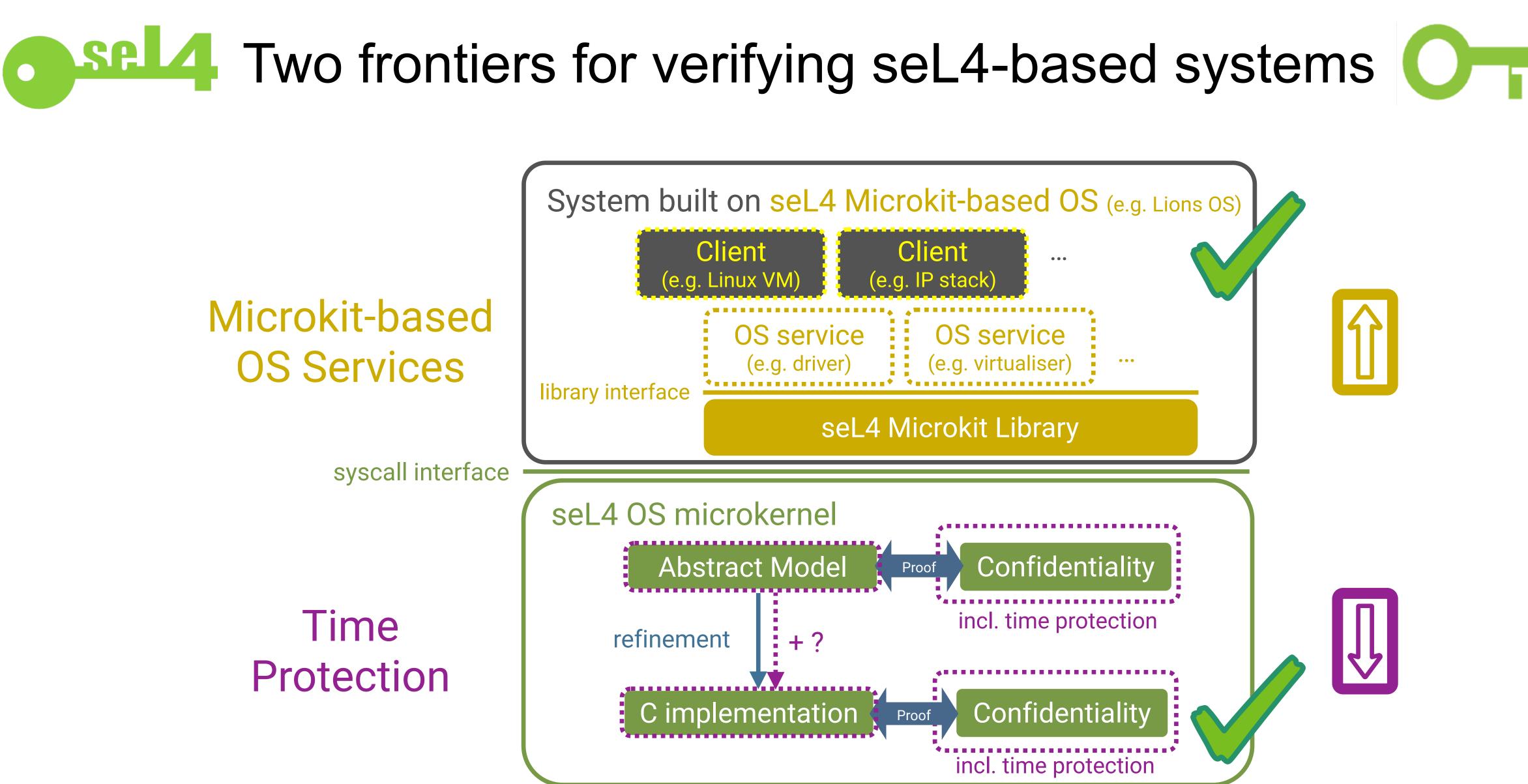


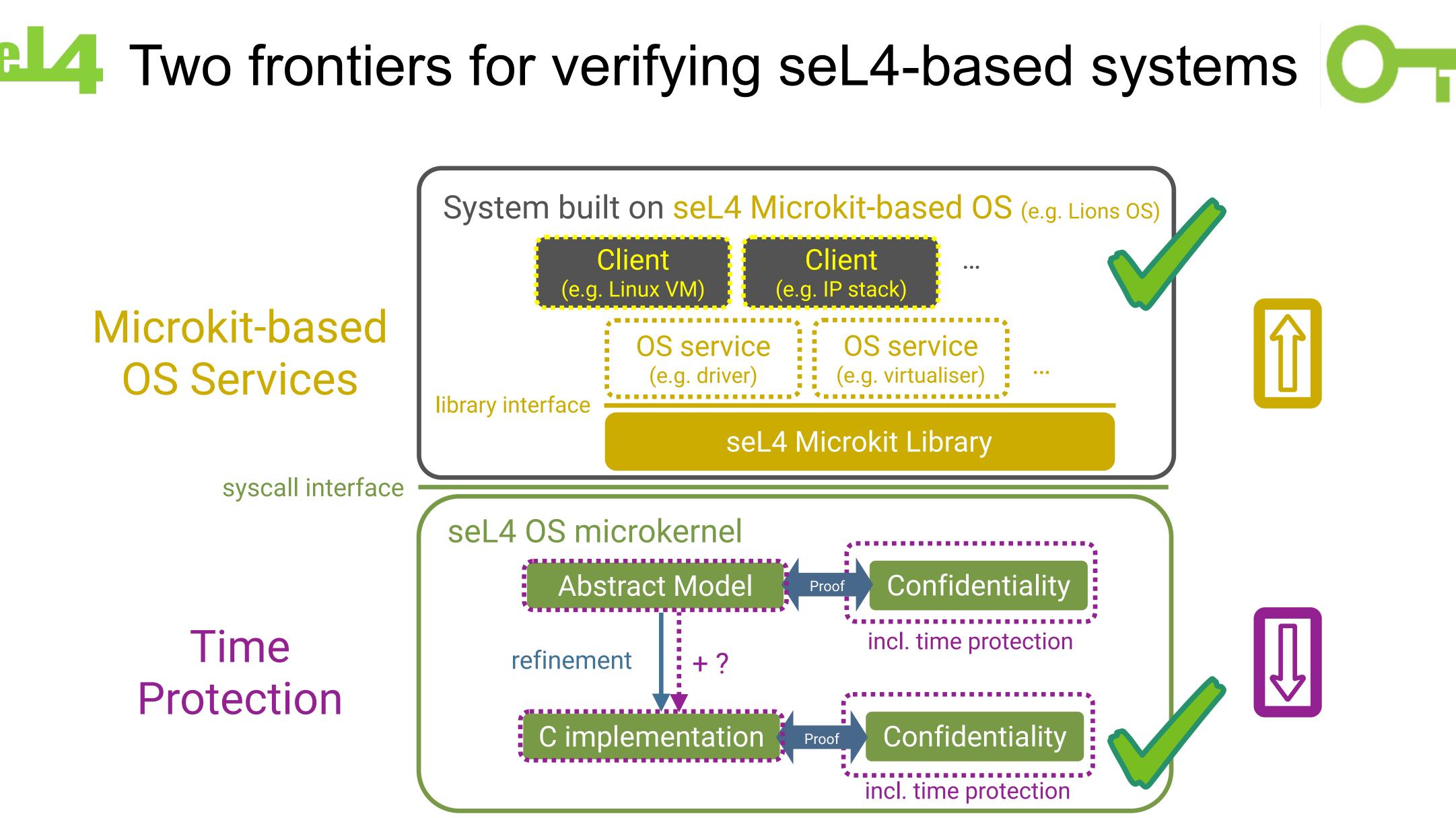










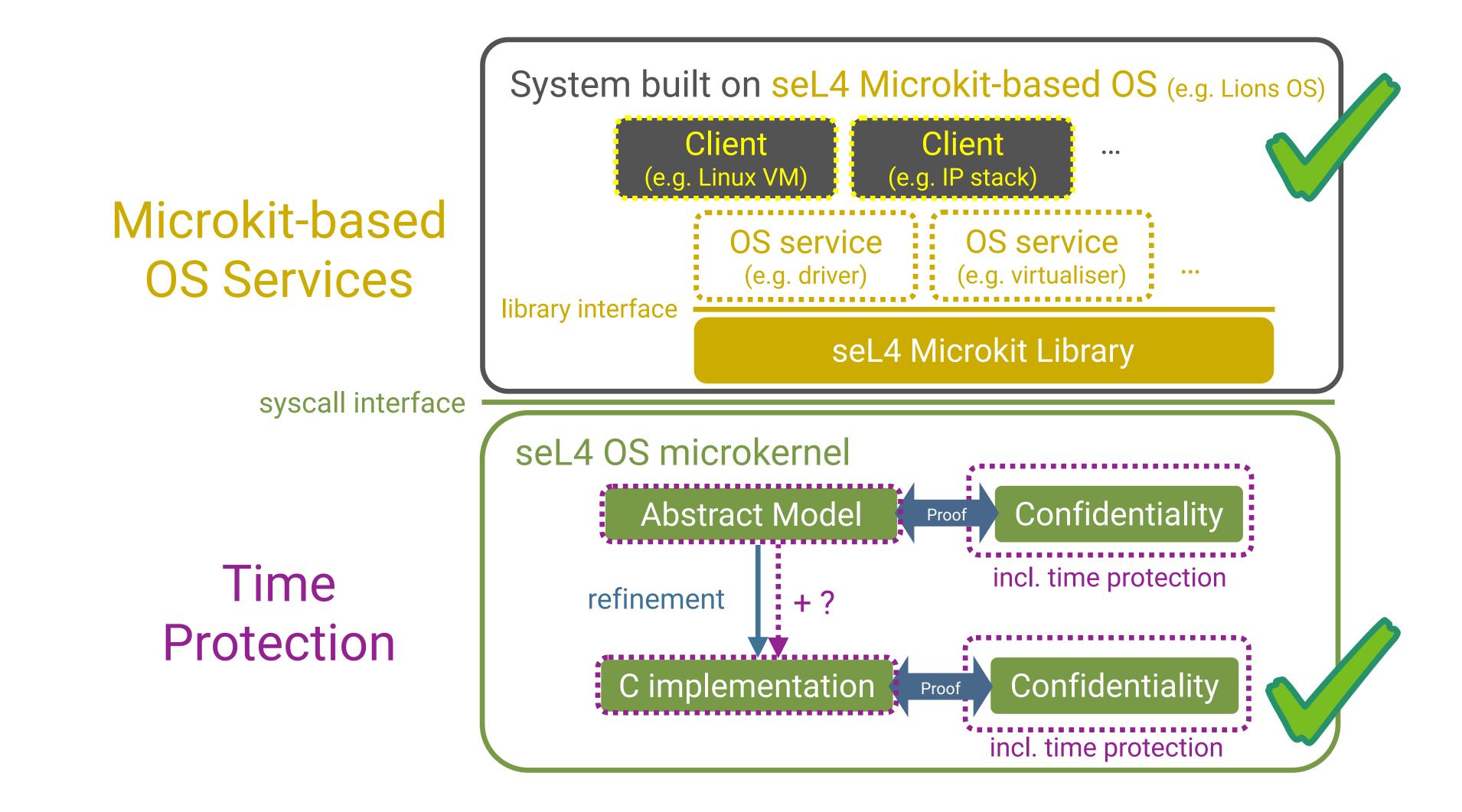












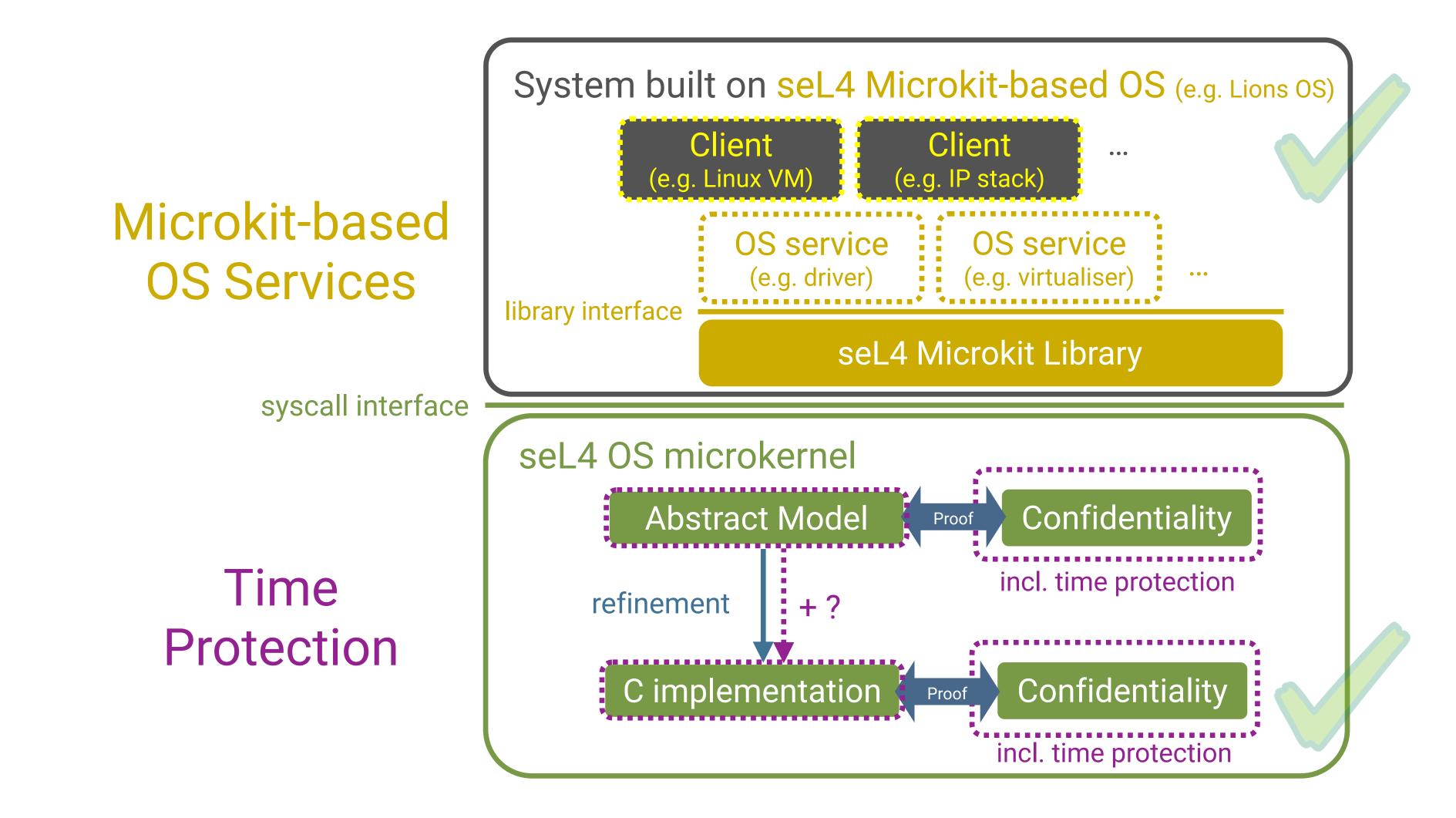
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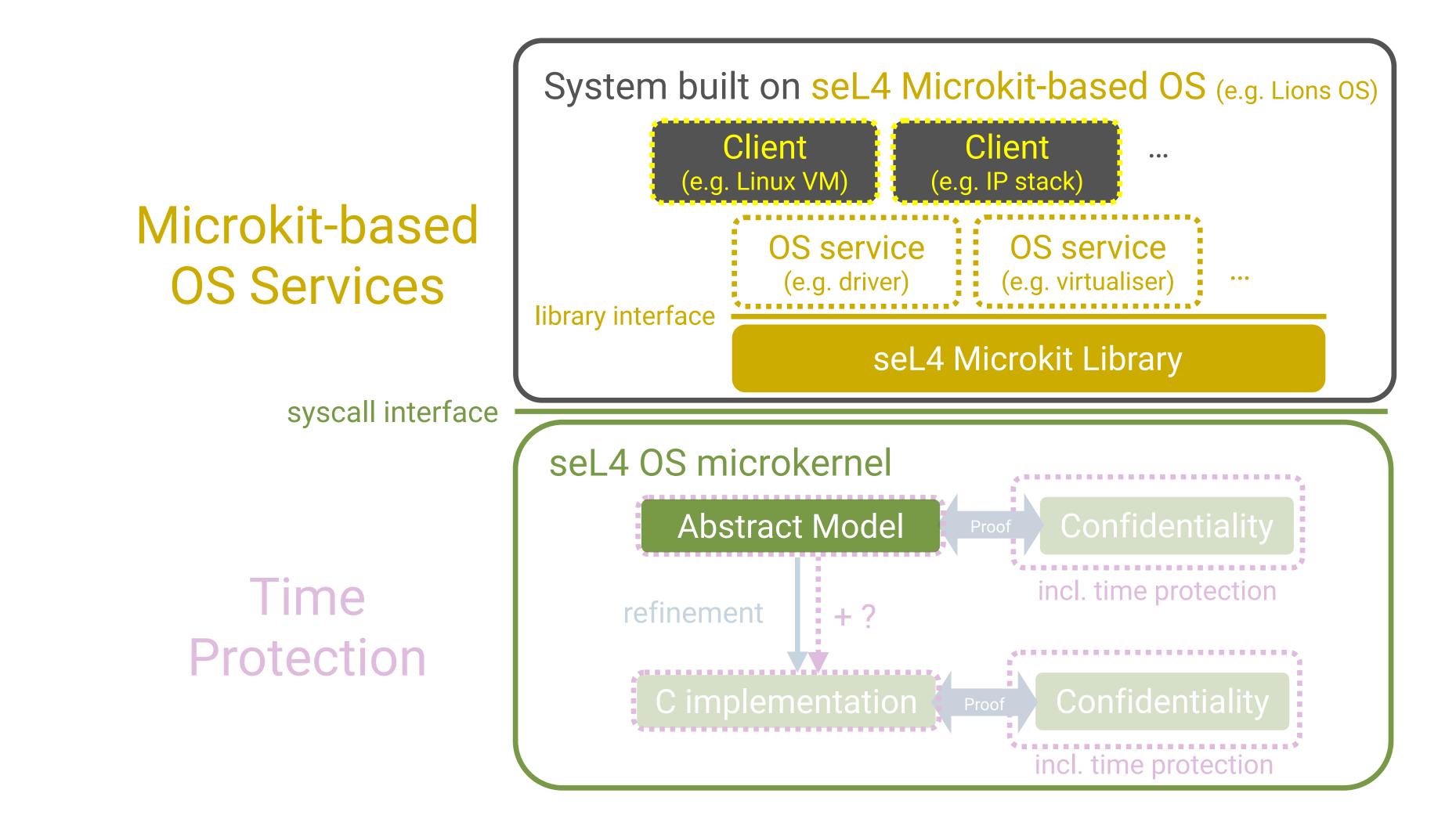
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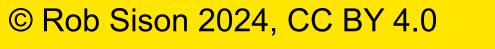






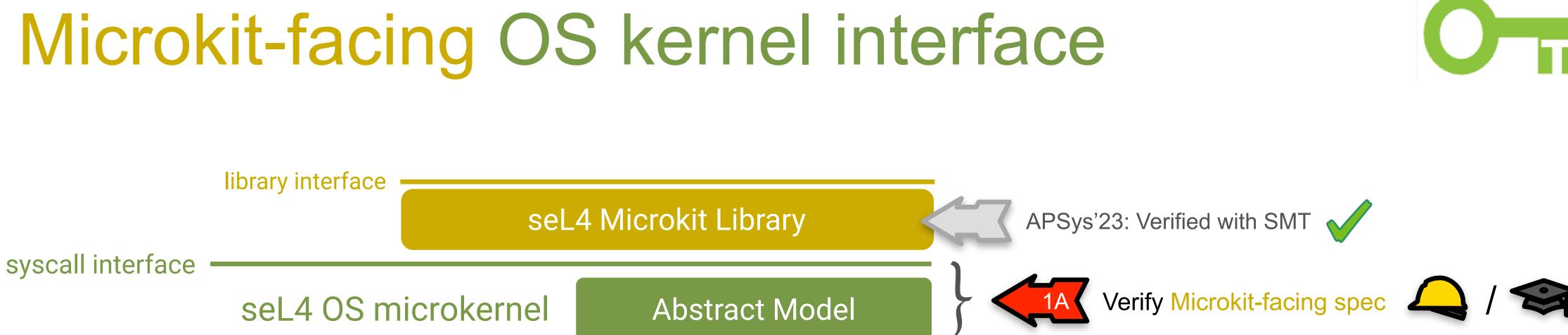
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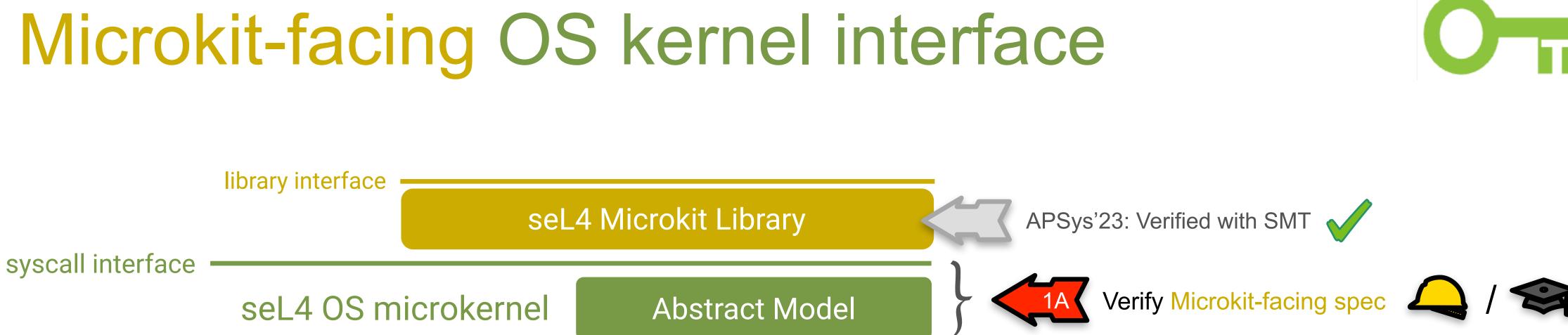


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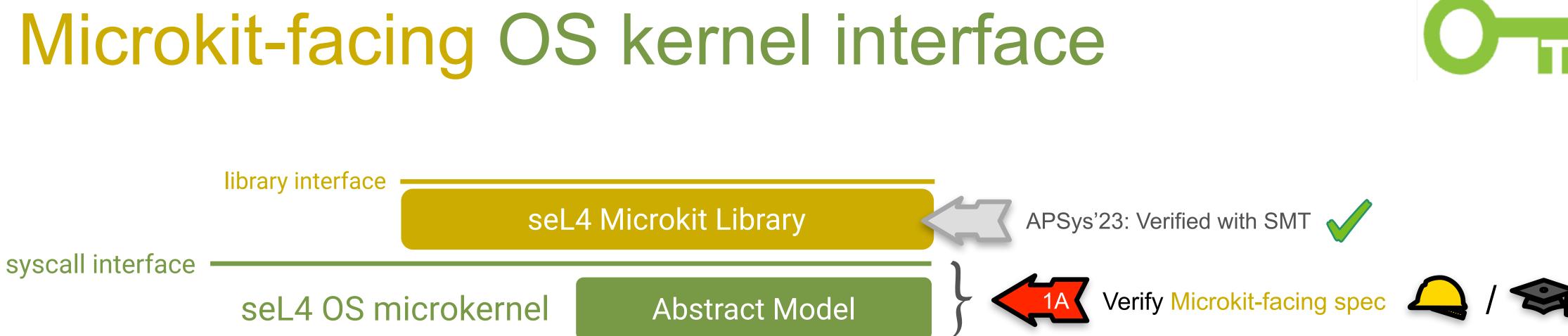
UNSW



Non-blocking cases: Straightforward

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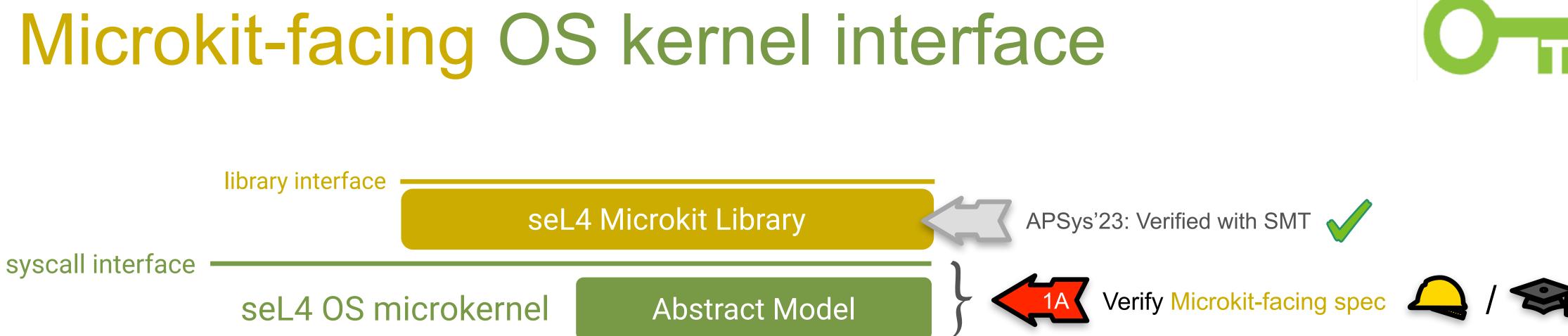




- Non-blocking cases: Straightforward
 - e.g. seL4_Recv returns immediately

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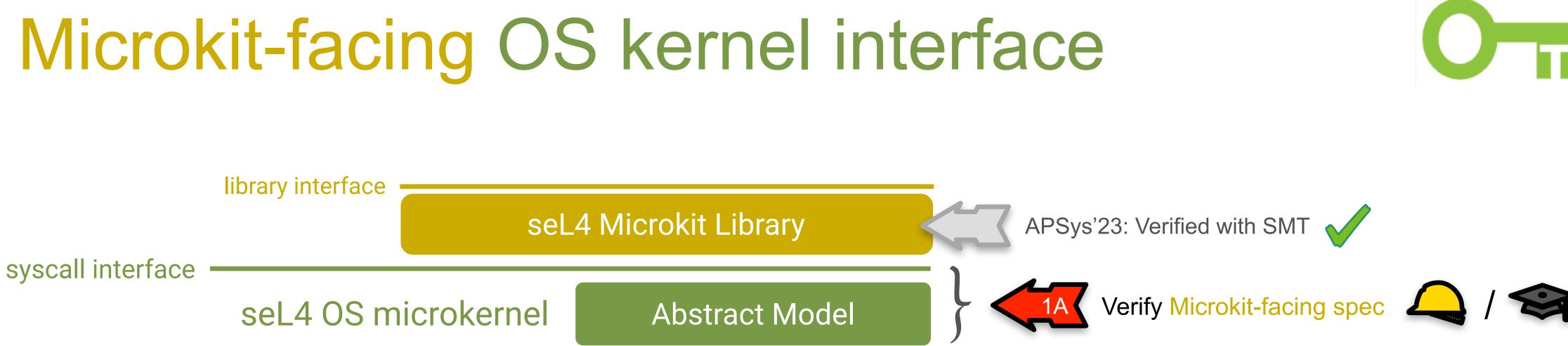




- Non-blocking cases: Straightforward
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 - Prove Hoare triple over single kernel entry/exit \bullet

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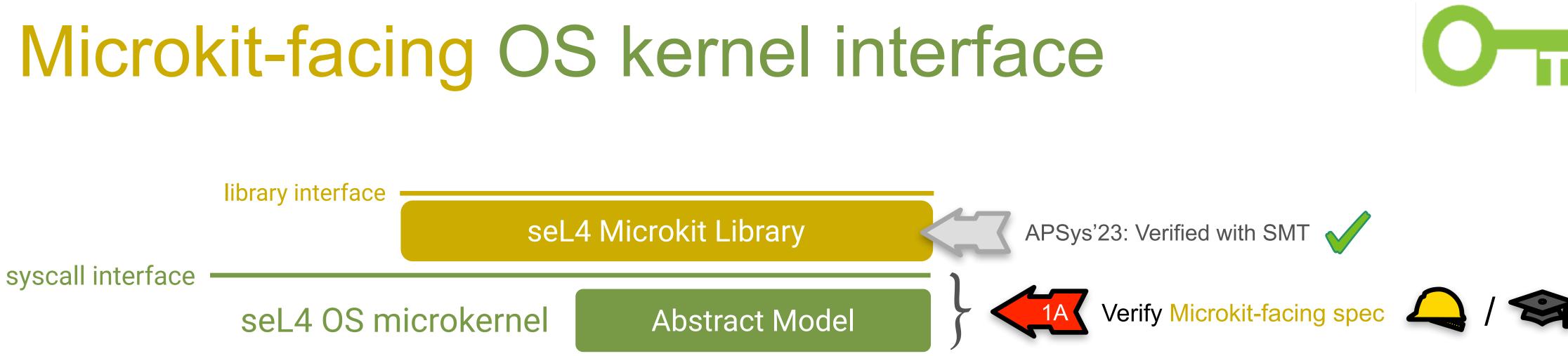


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Blocking cases: Tricky ullet

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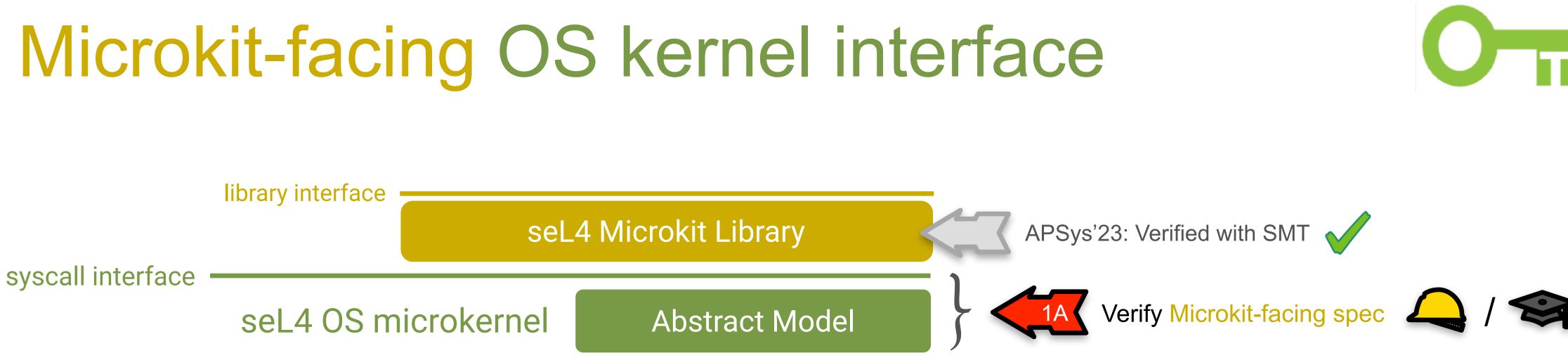
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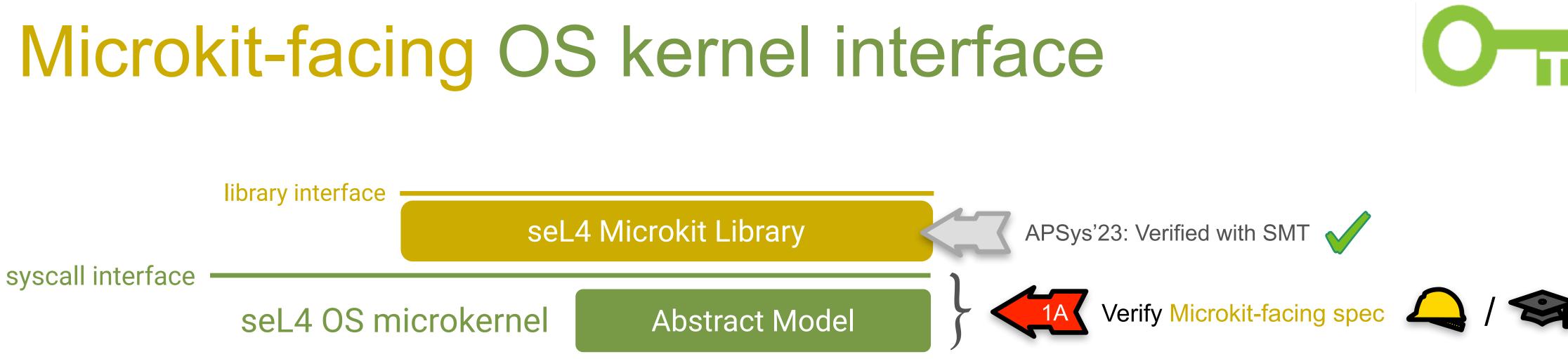


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- Blocking cases: Tricky \bullet
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 - Kernel returns to different user! ... Caller is woken by seL4 Call later.





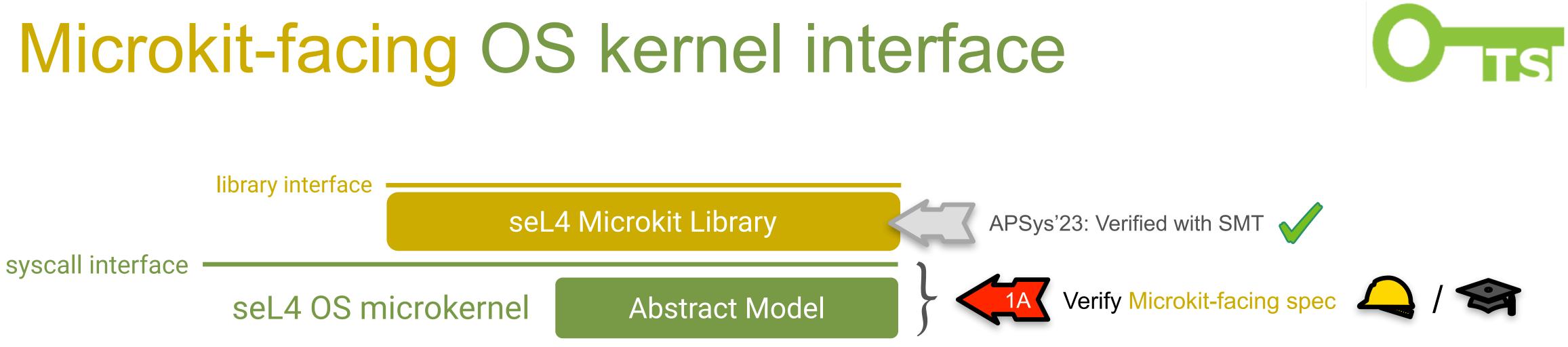


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 - cf. CertiKOS ESOP'20 blocks on IO, not another user







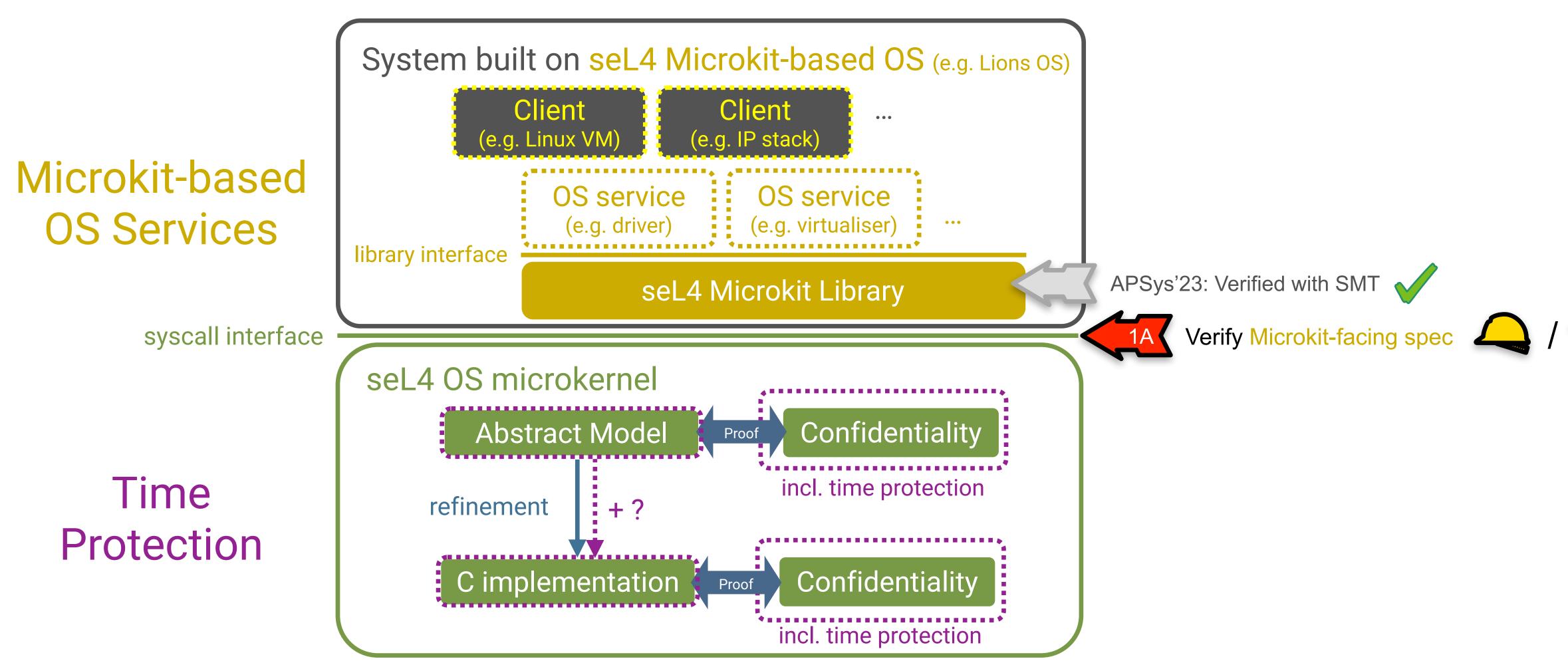
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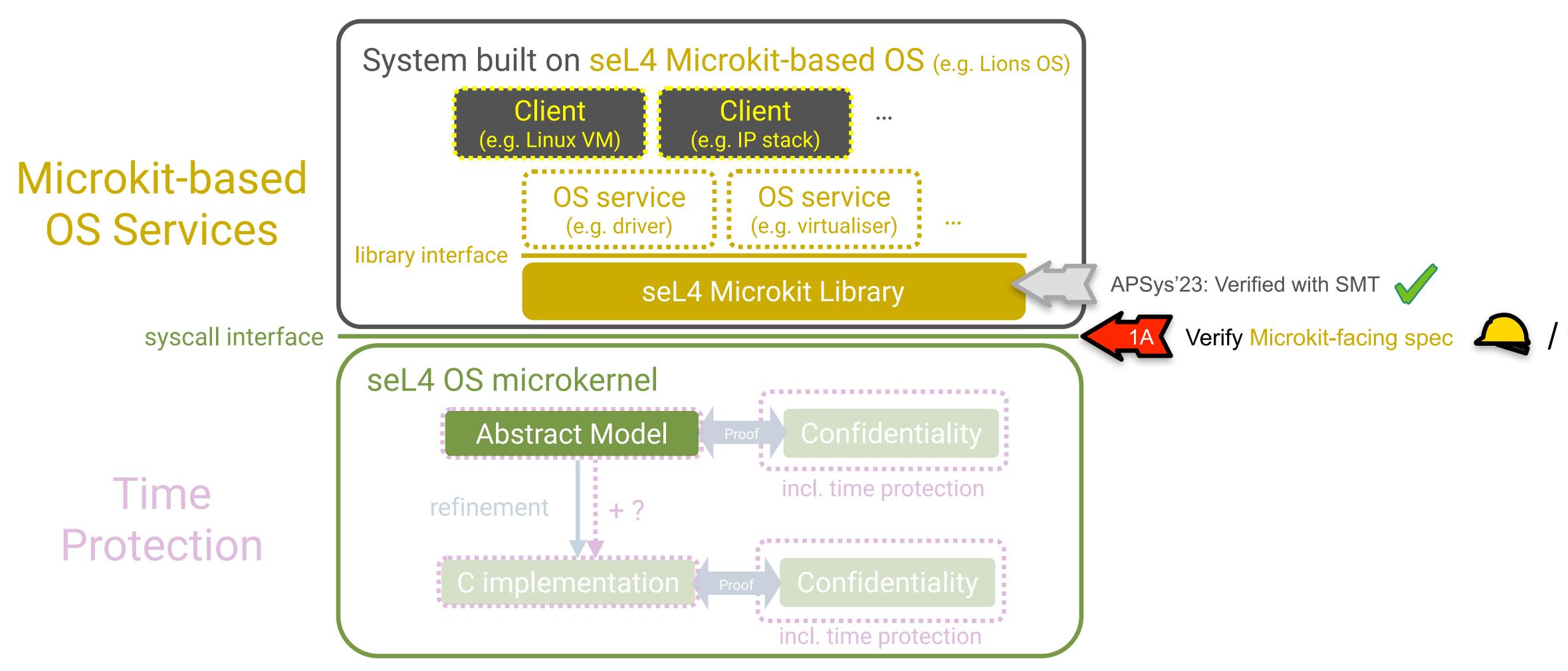












Verification Status of Time Protection and Microkit-based OS Services, Oct'24



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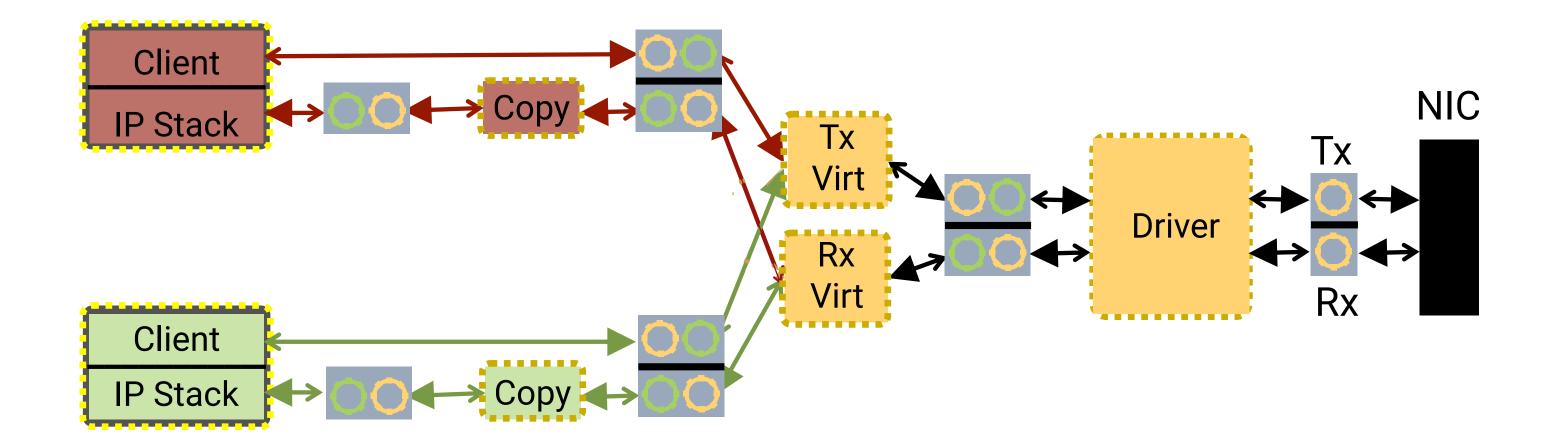




Microkit-based OS services, drivers (+ devices)

Ethernet virtualisation architecture for







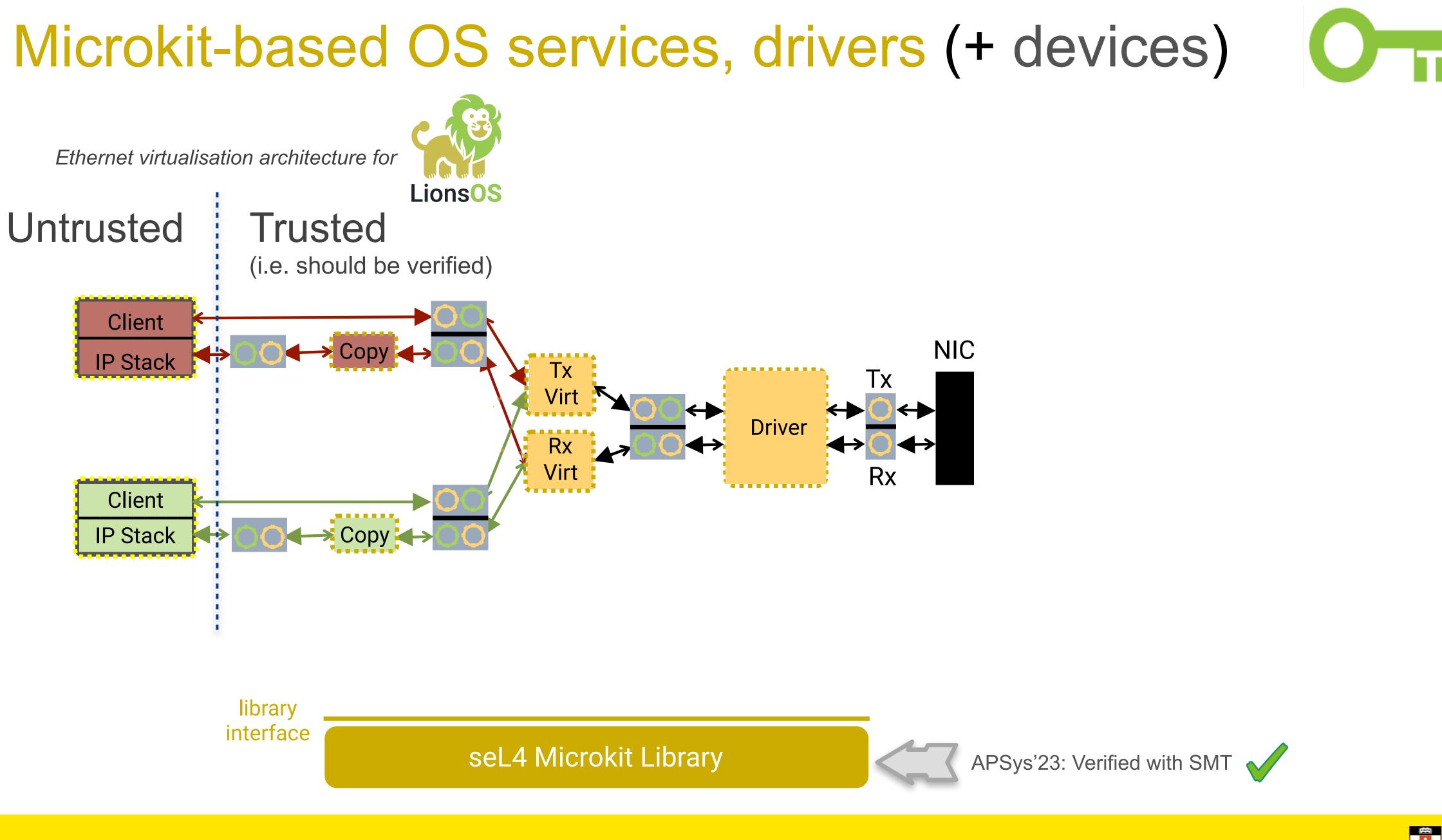
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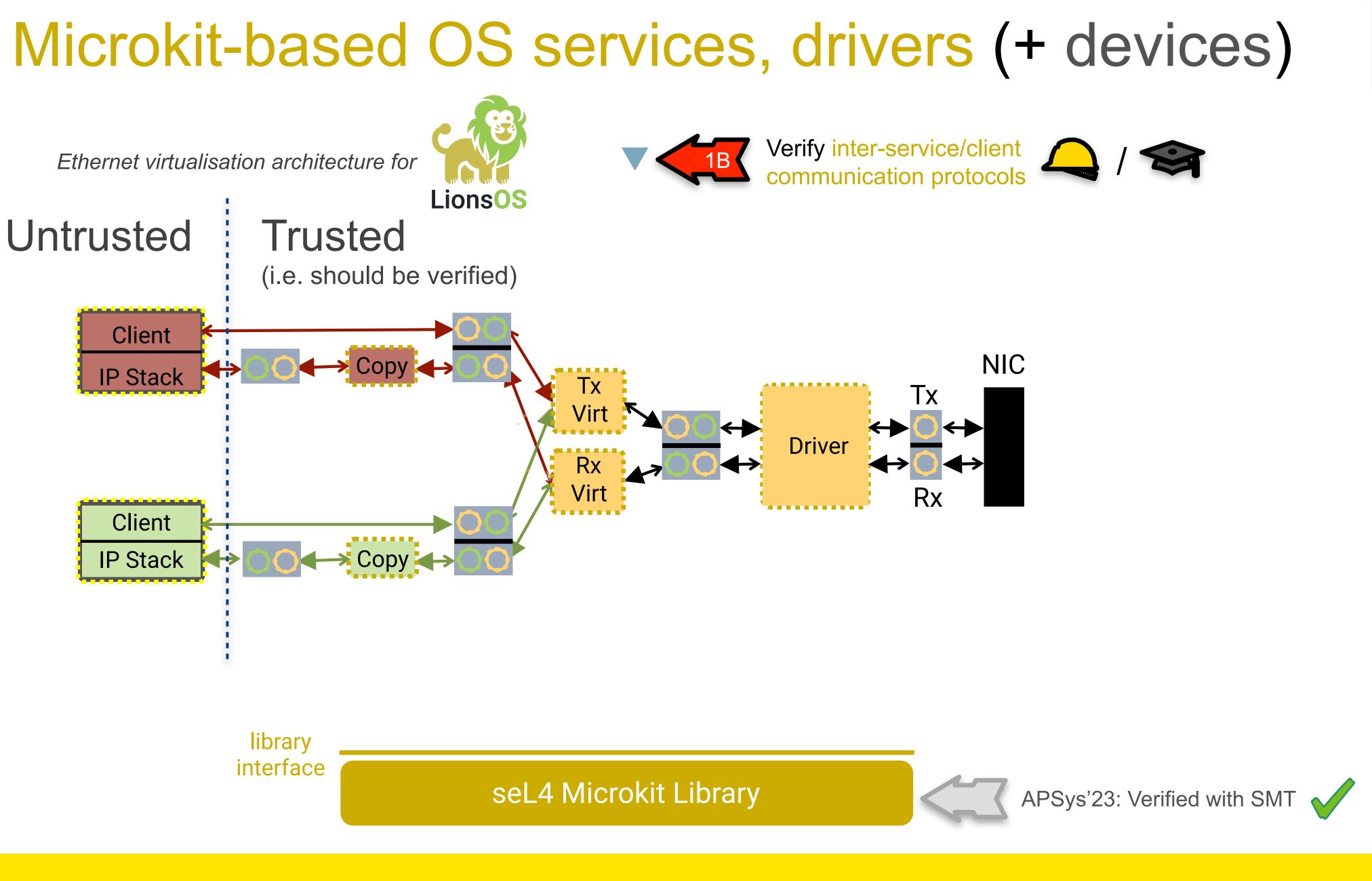






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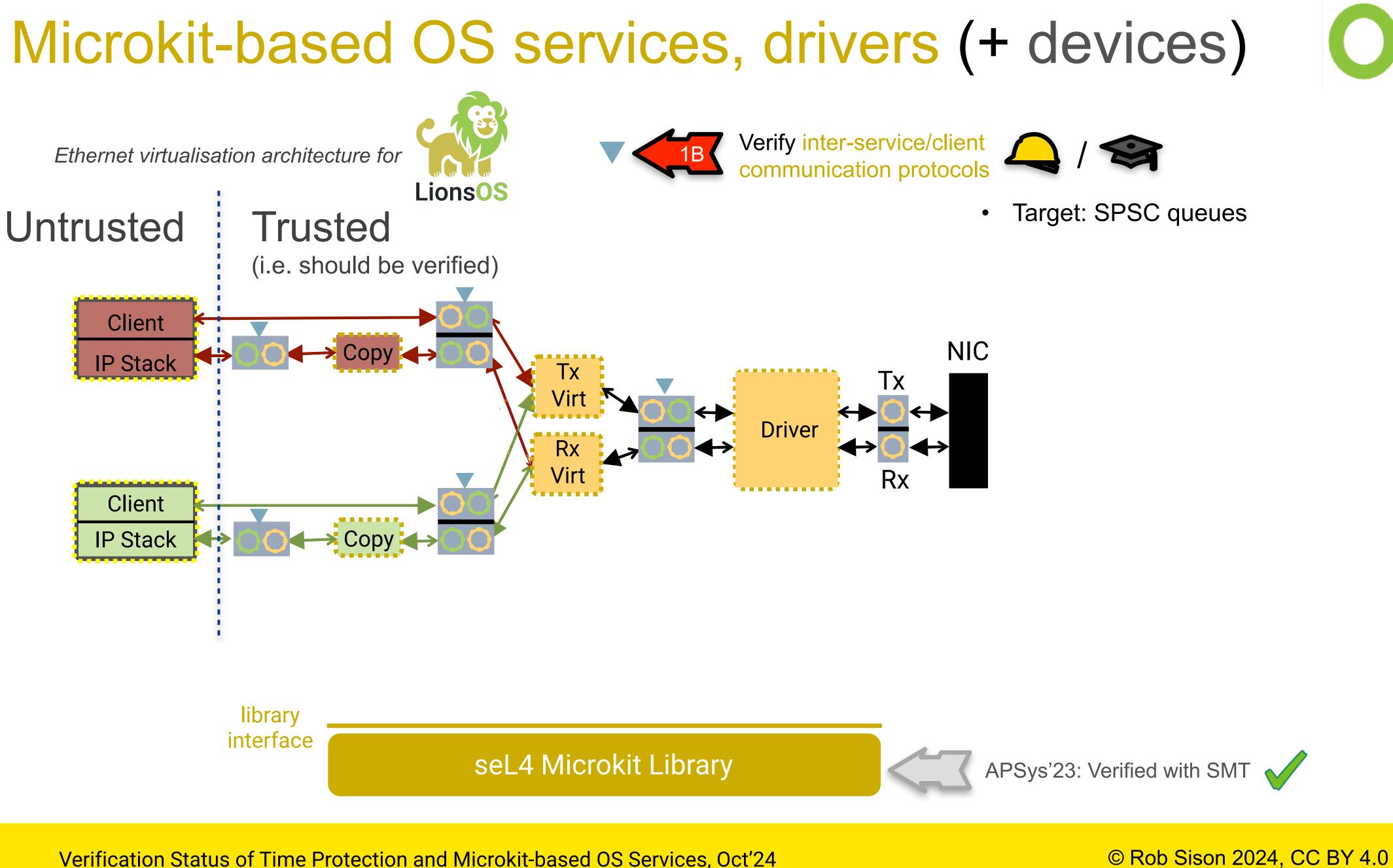






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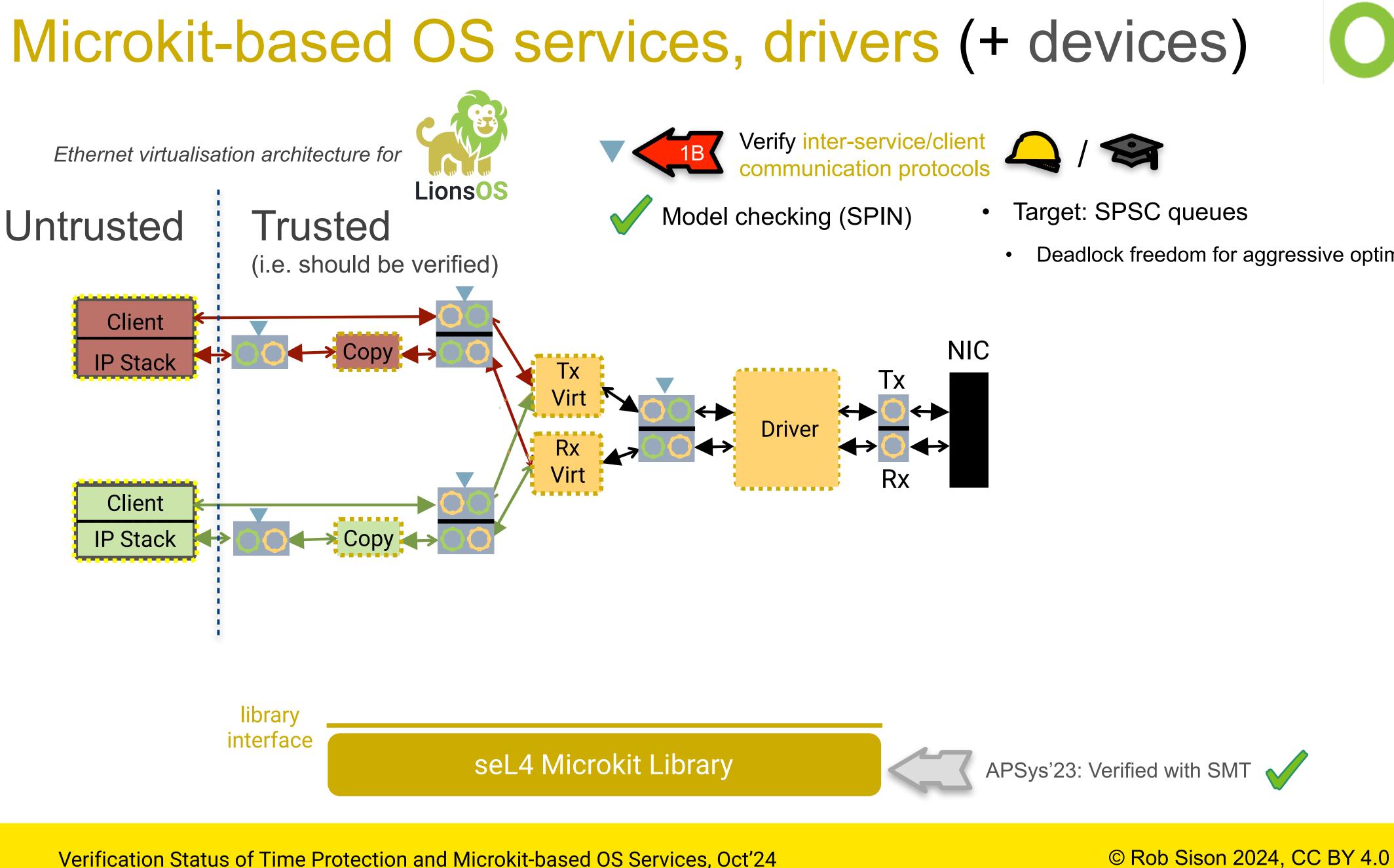














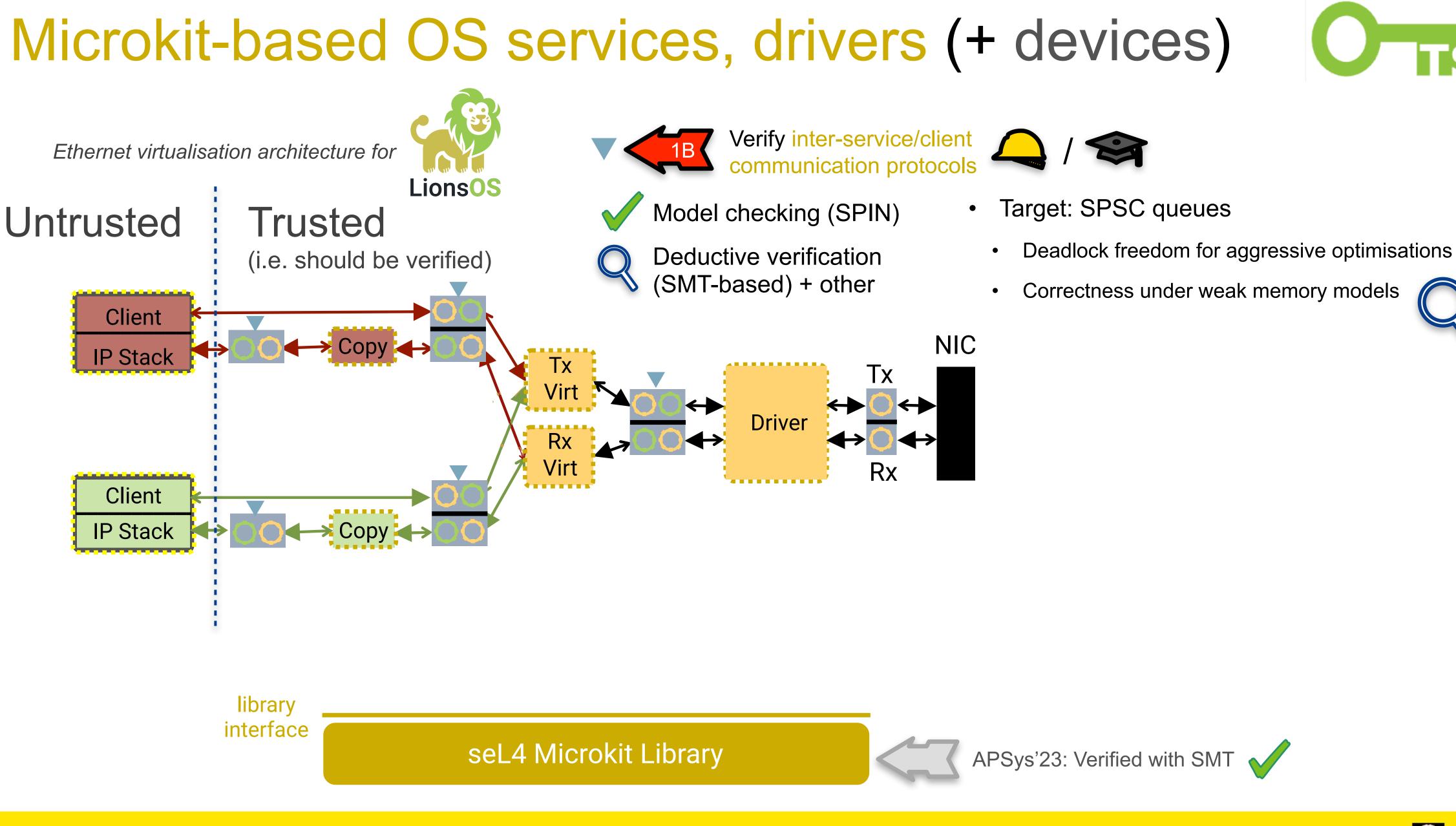


- - Deadlock freedom for aggressive optimisations













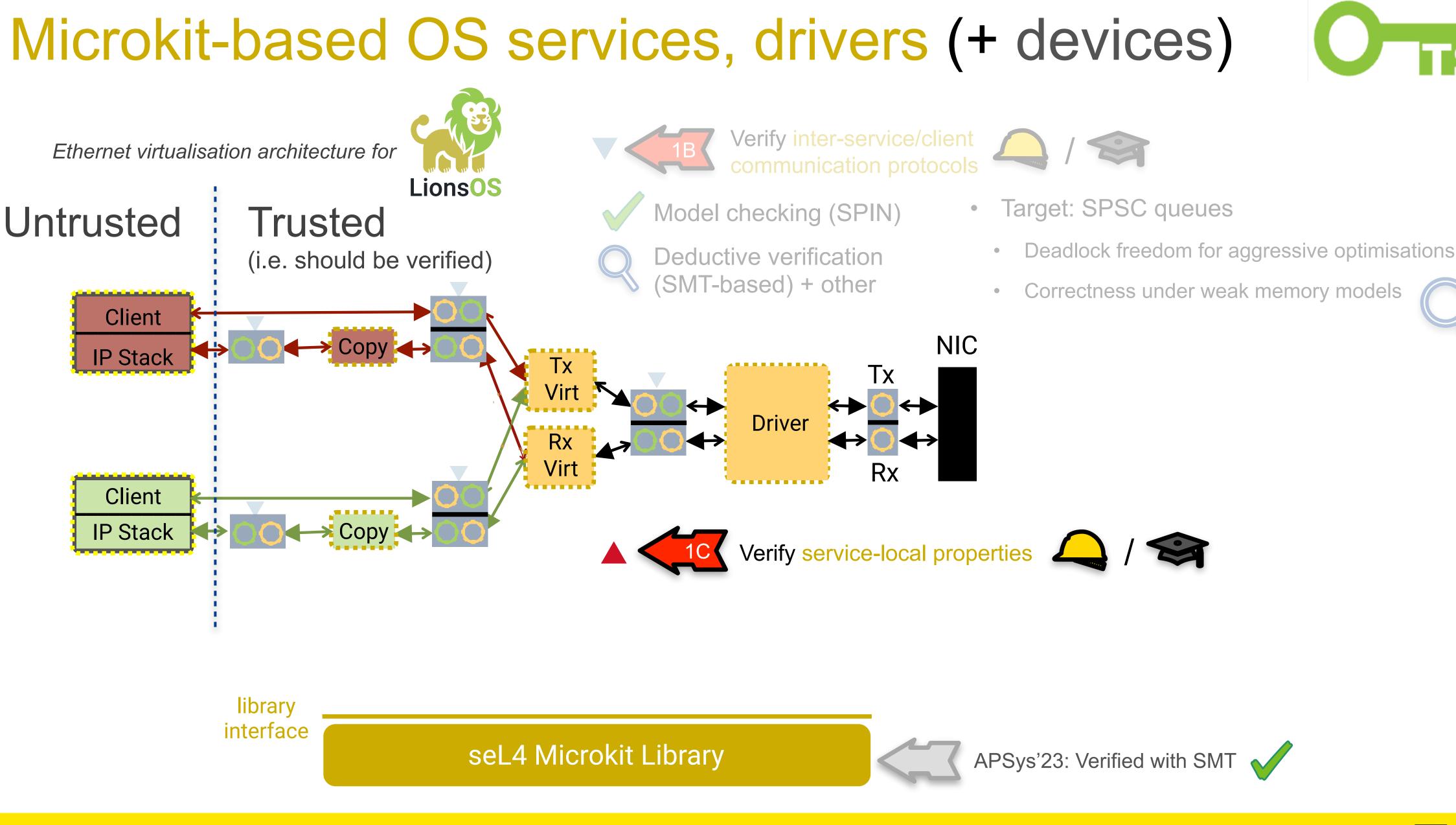
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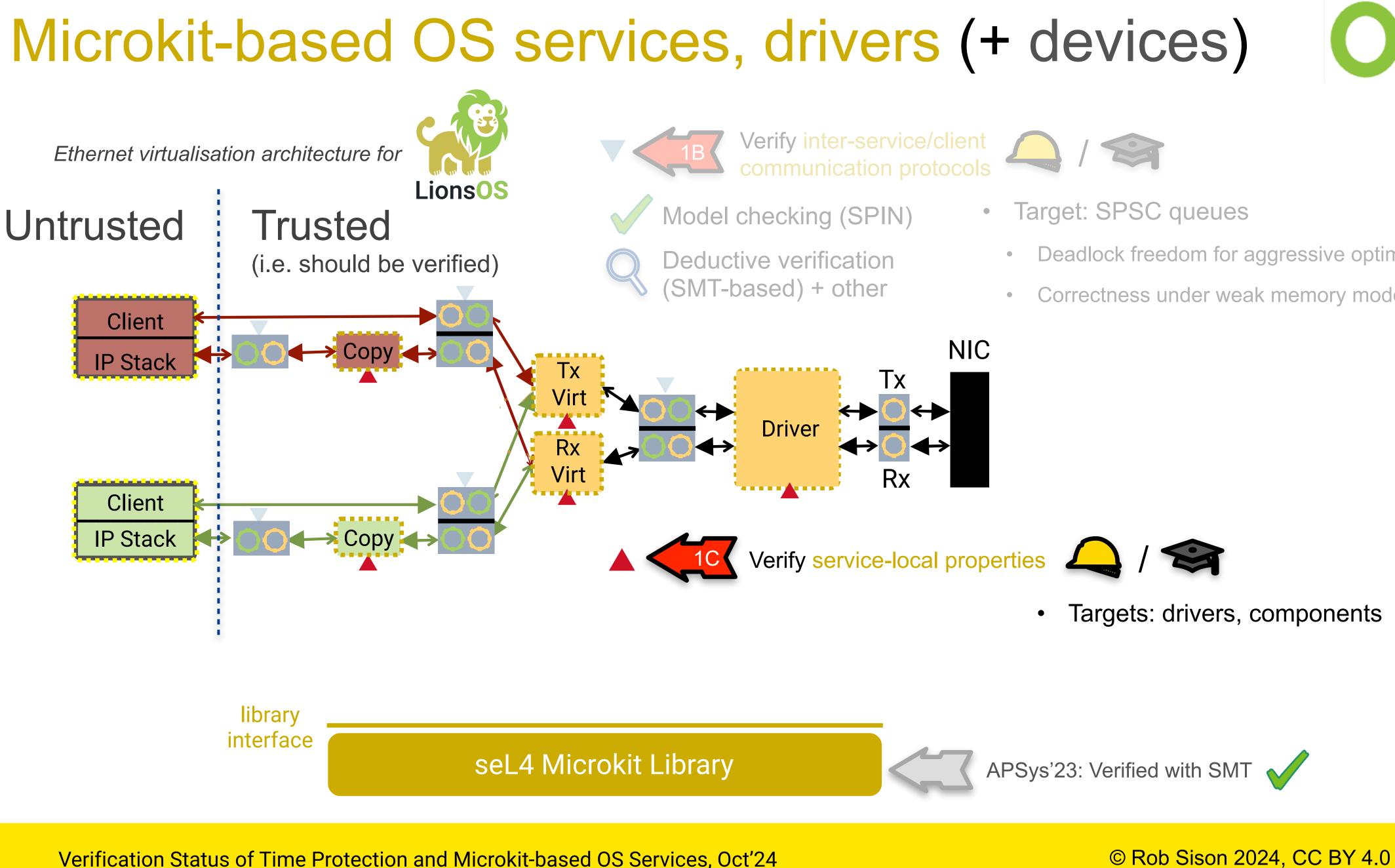


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- - Deadlock freedom for aggressive optimisations
 - Correctness under weak memory models

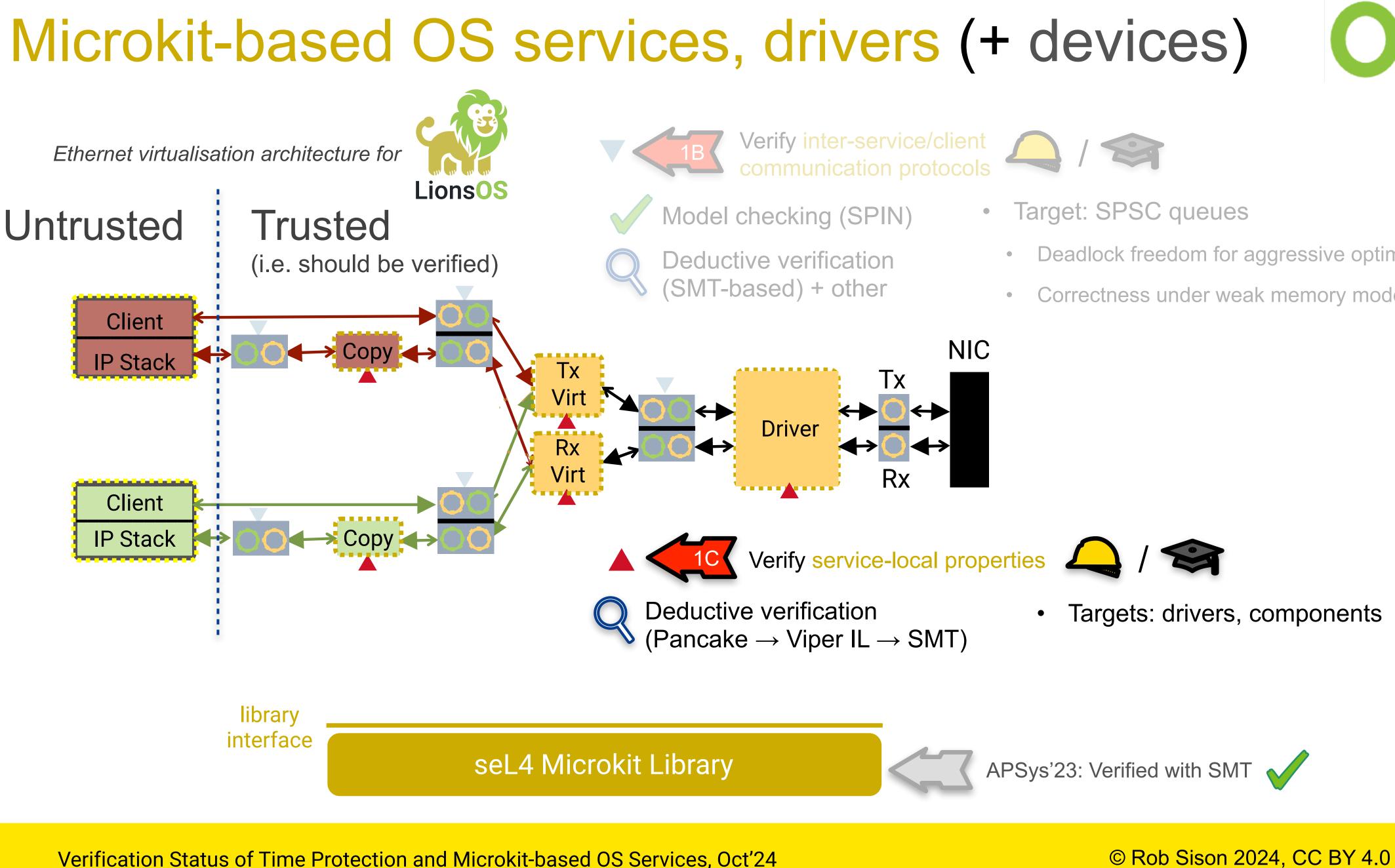




Targets: drivers, components











- - Deadlock freedom for aggressive optimisations
 - Correctness under weak memory models

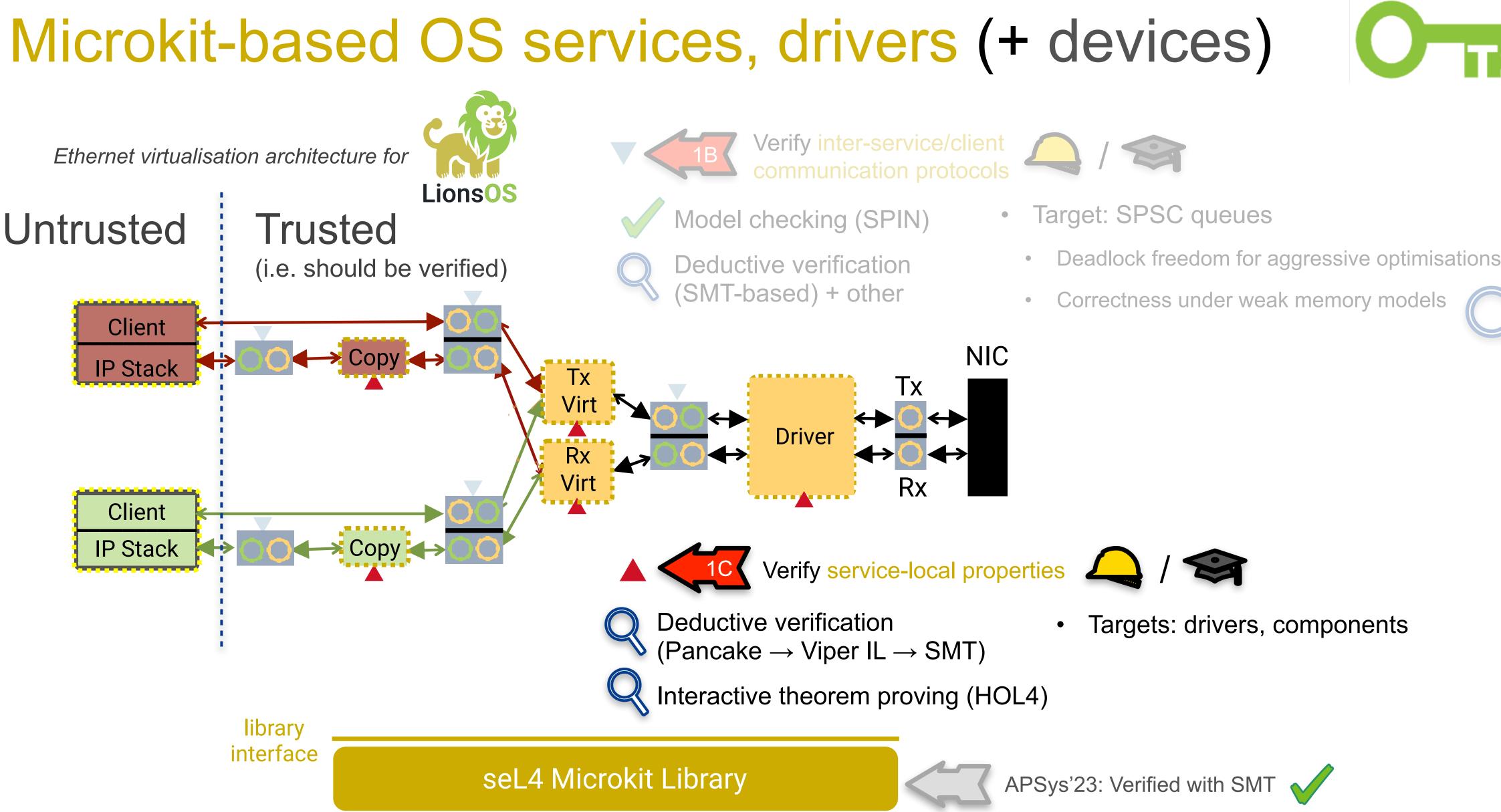




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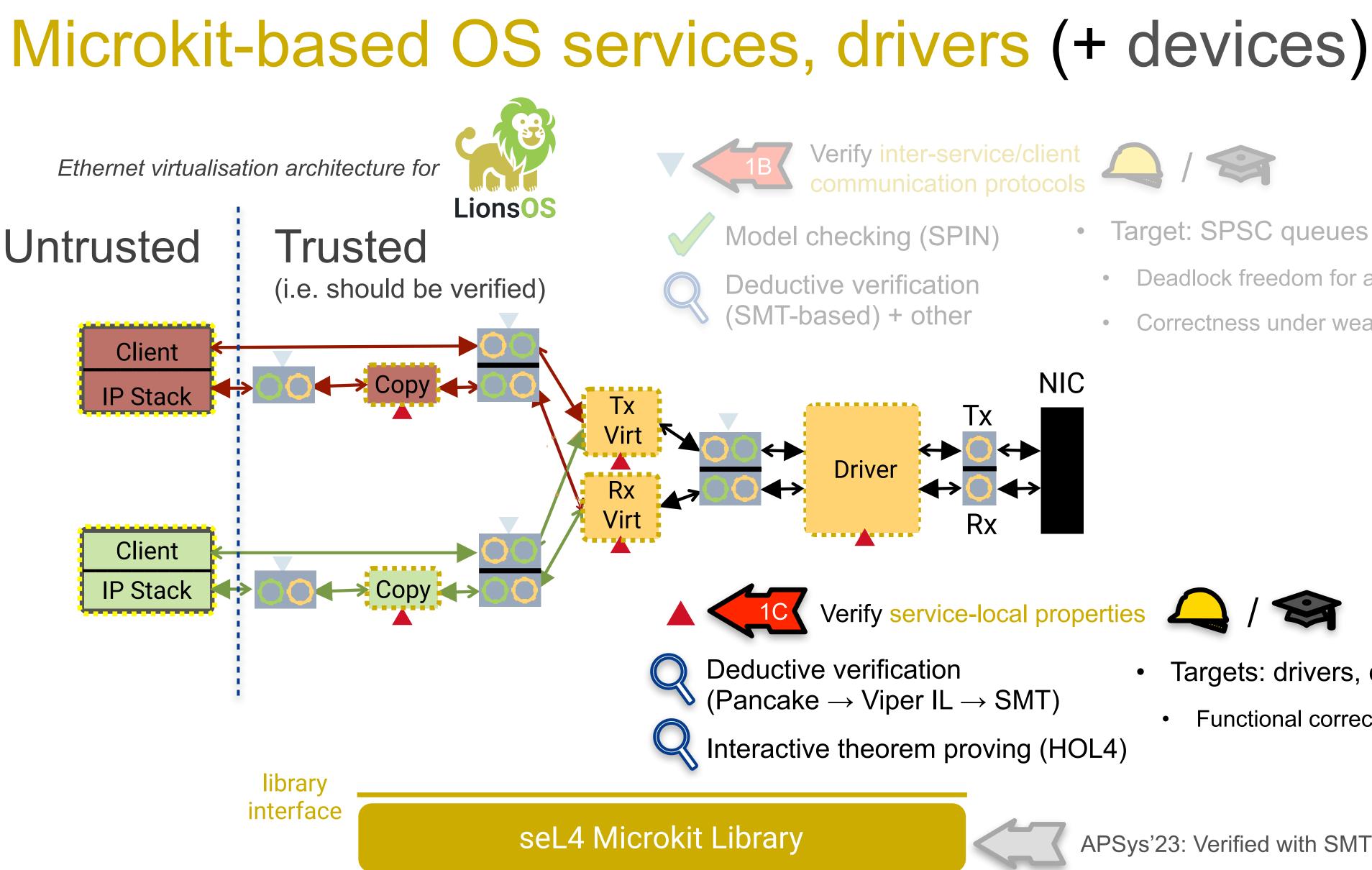


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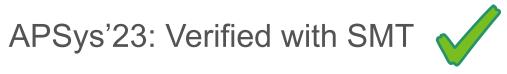




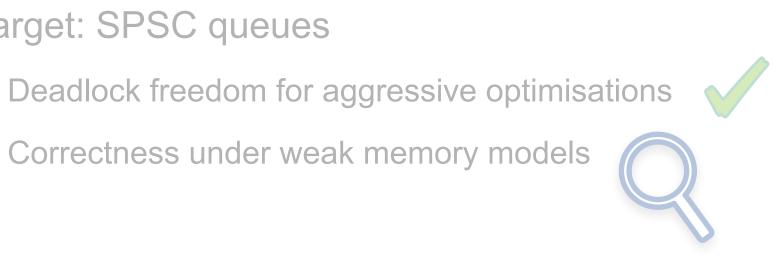
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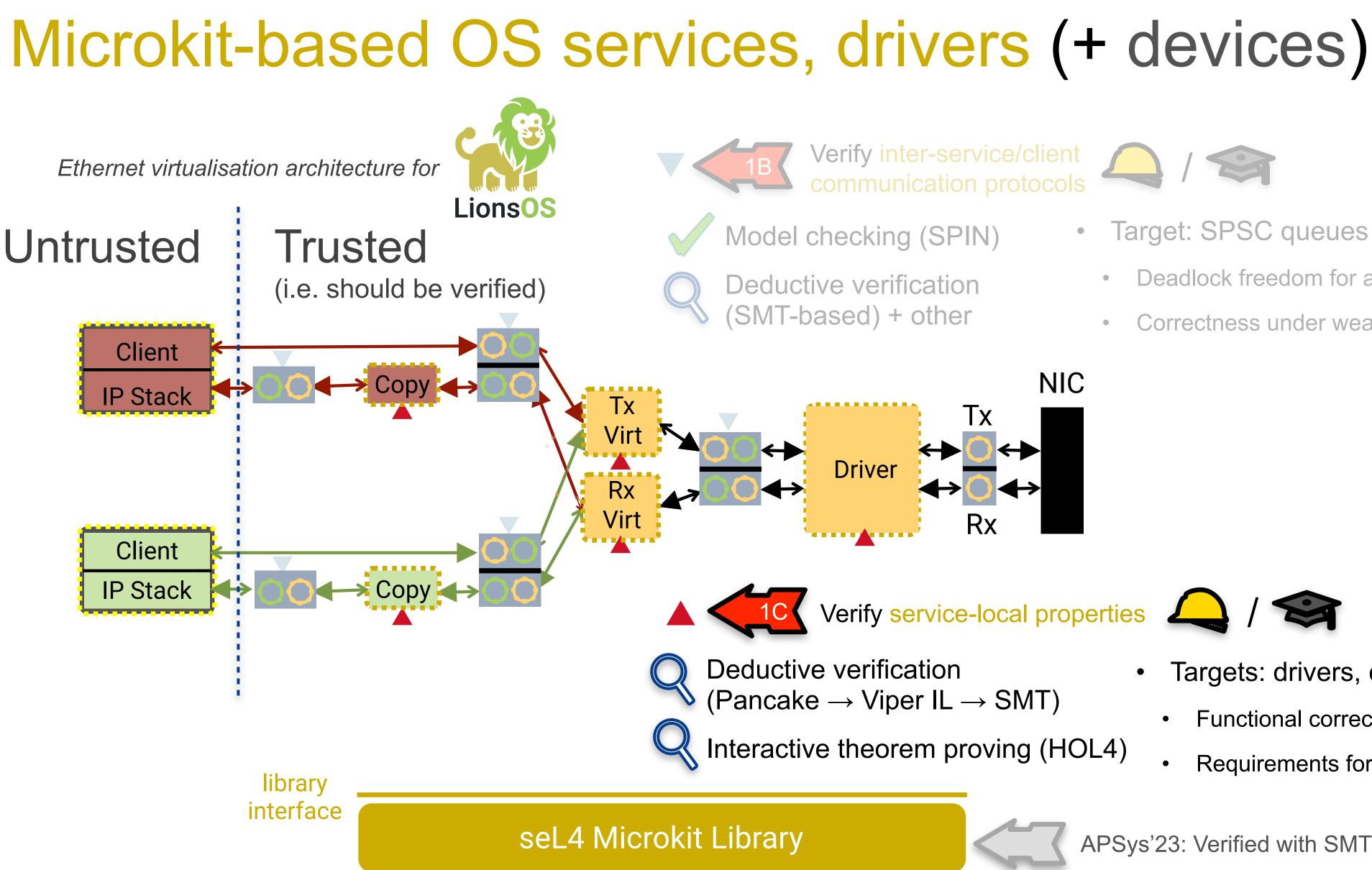
Correctness under weak memory models

Functional correctness













- Deadlock freedom for aggressive optimisations
- Correctness under weak memory models



- Targets: drivers, components
- **Functional correctness**
- Requirements for device verification

APSys'23: Verified with SMT

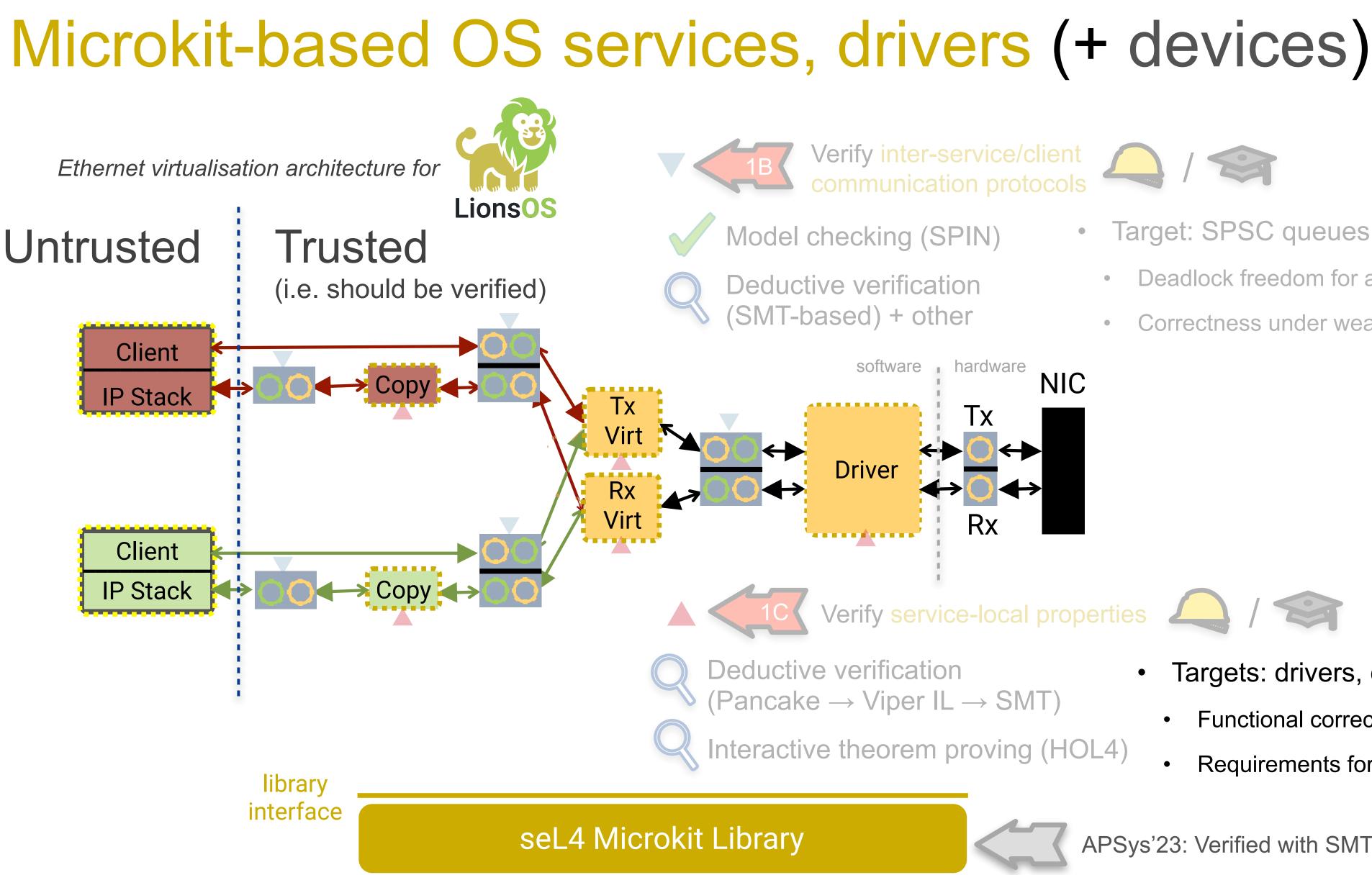
















- Target: SPSC queues
 - Deadlock freedom for aggressive optimisations
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APSys'23: Verified with SMT



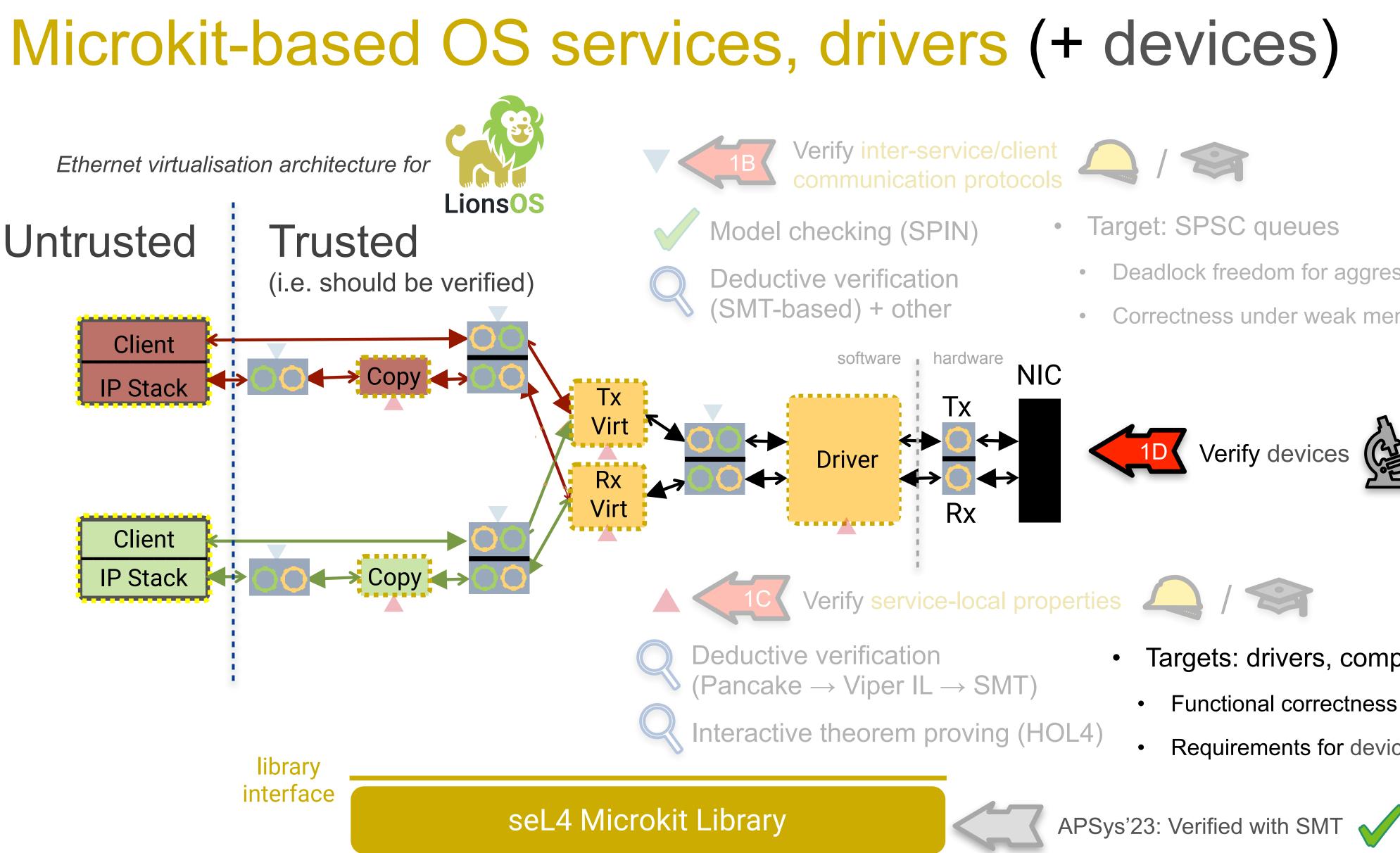


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- Deadlock freedom for aggressive optimisations
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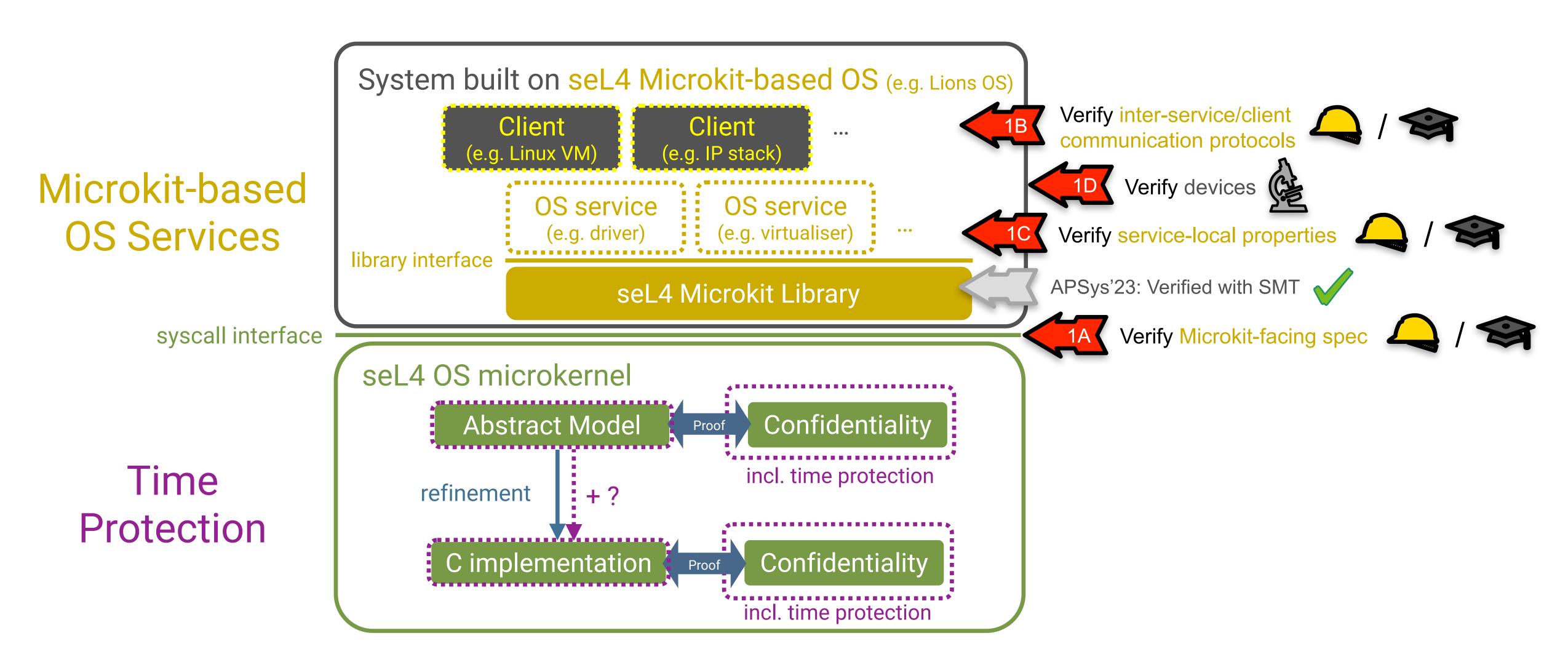








Verification status





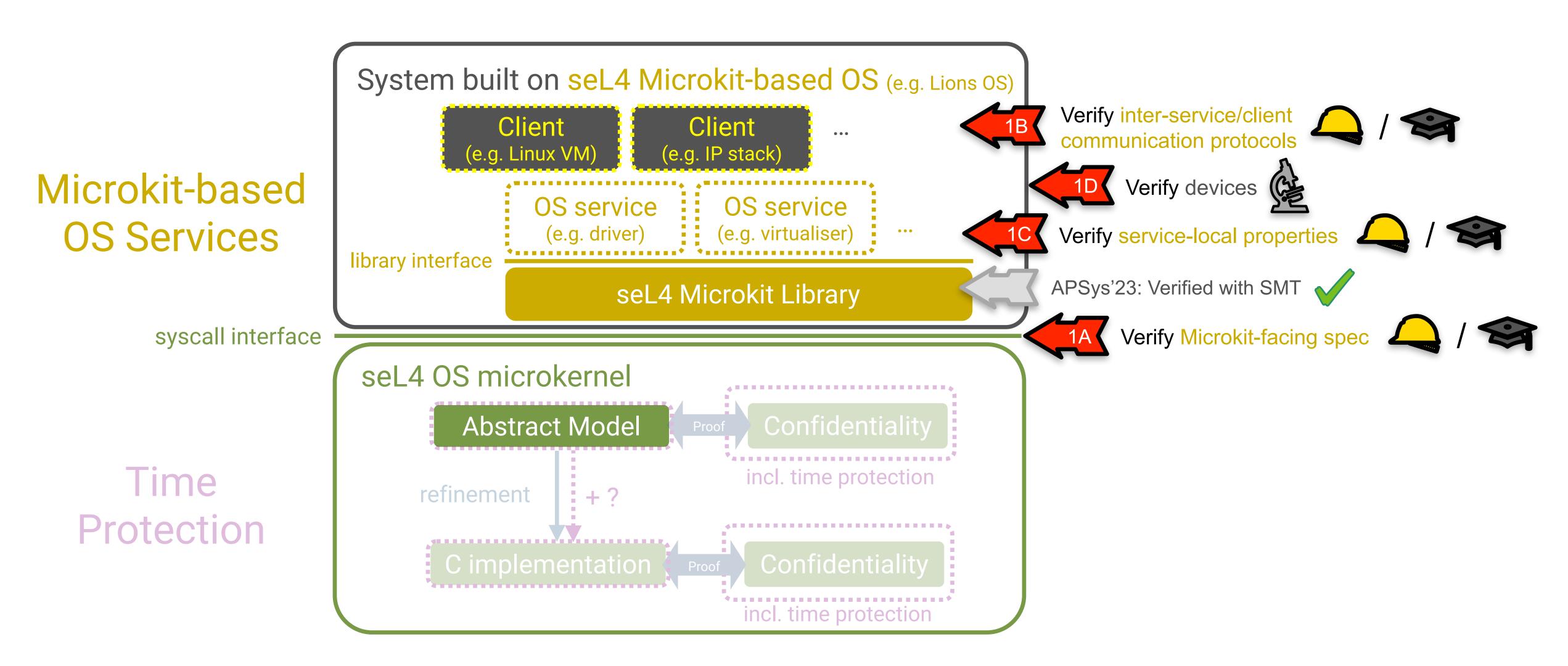








Verification status



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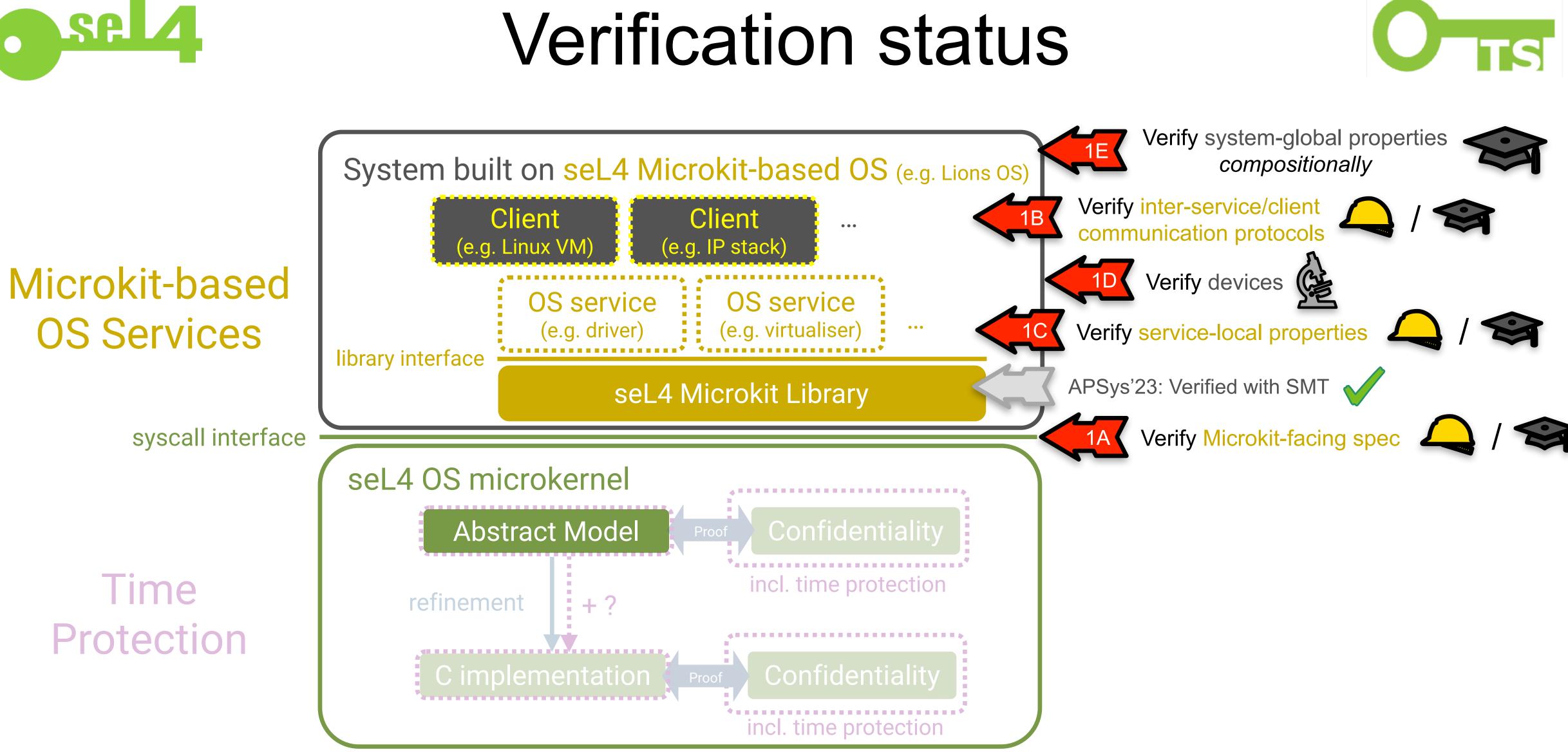












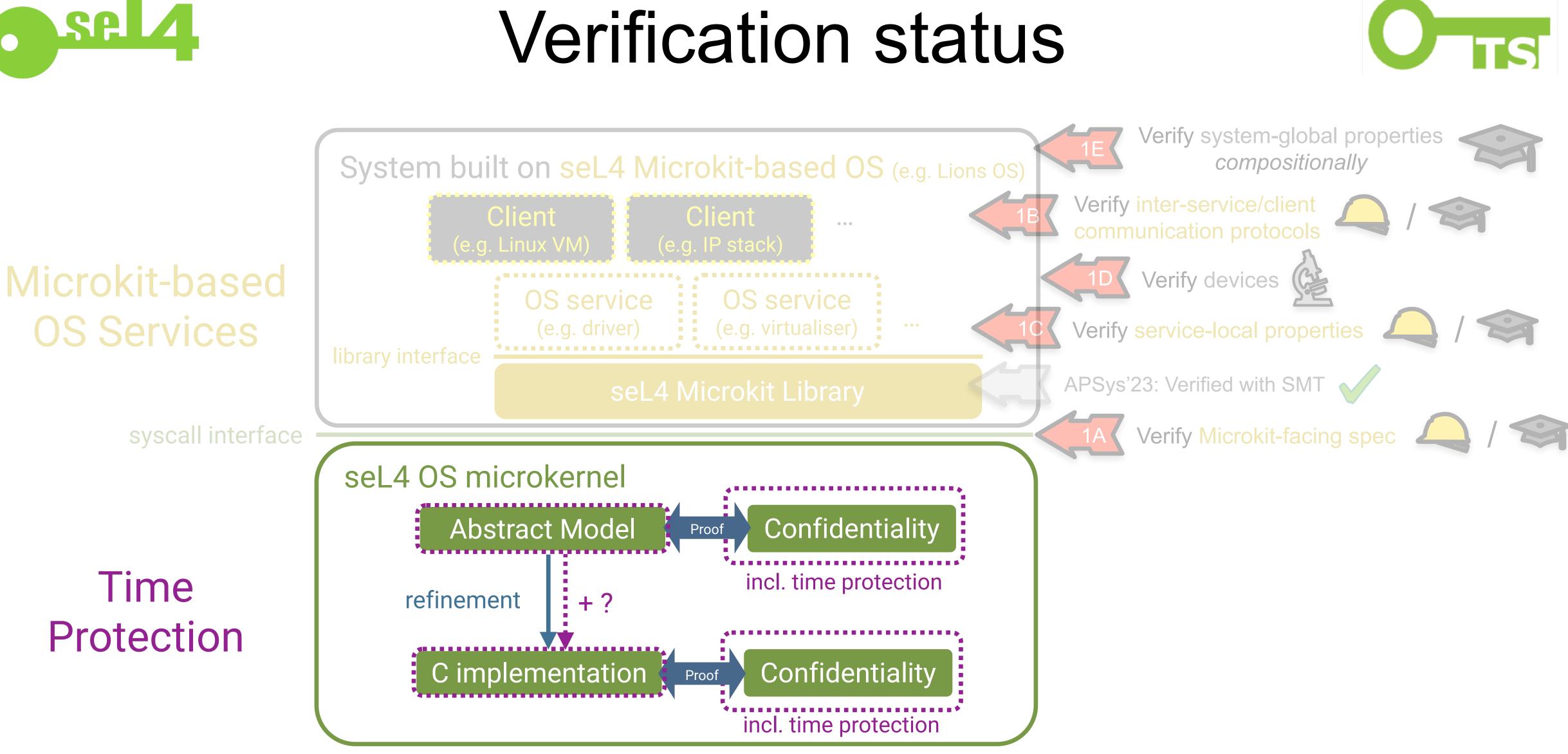
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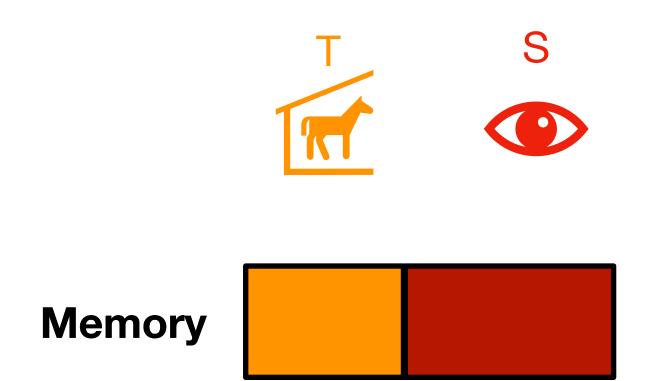












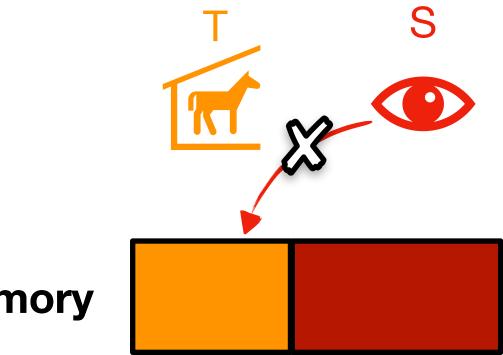
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OSes typically implement *memory protection*. lacksquare





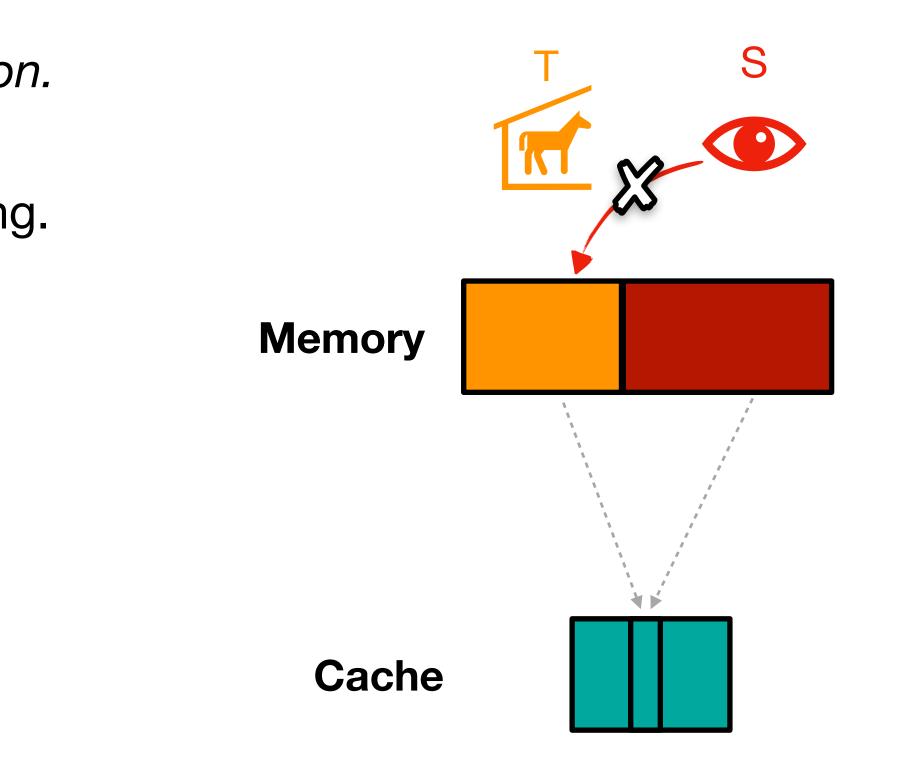
Memory





- OSes typically implement *memory protection*.
- But: Mere memory access changes \bullet microarchitectural state — this affects timing.





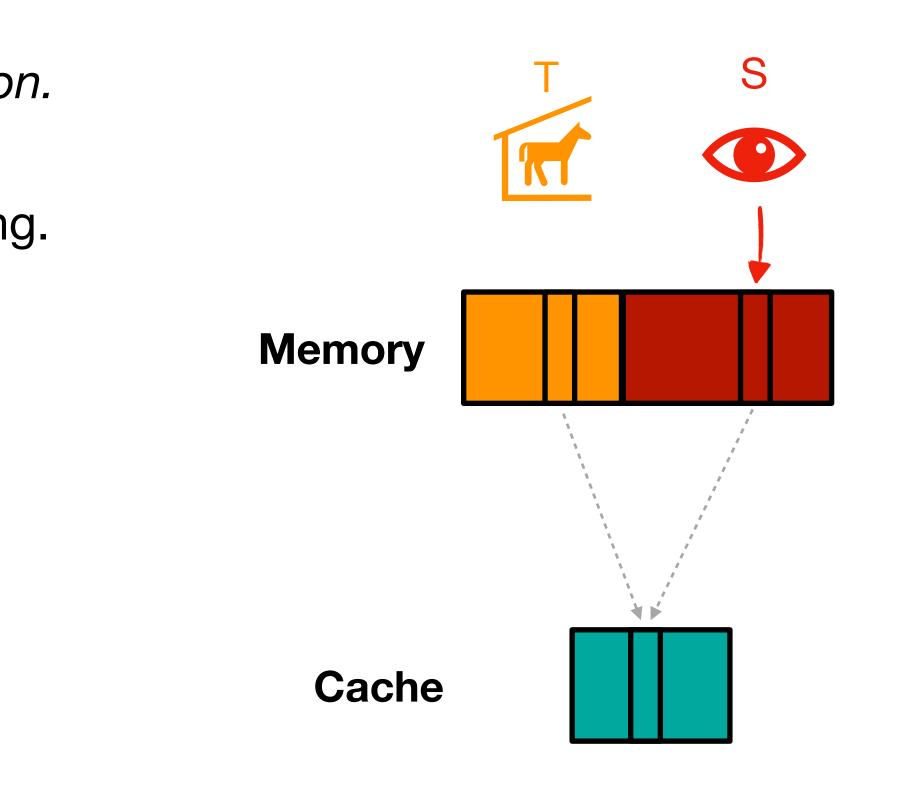


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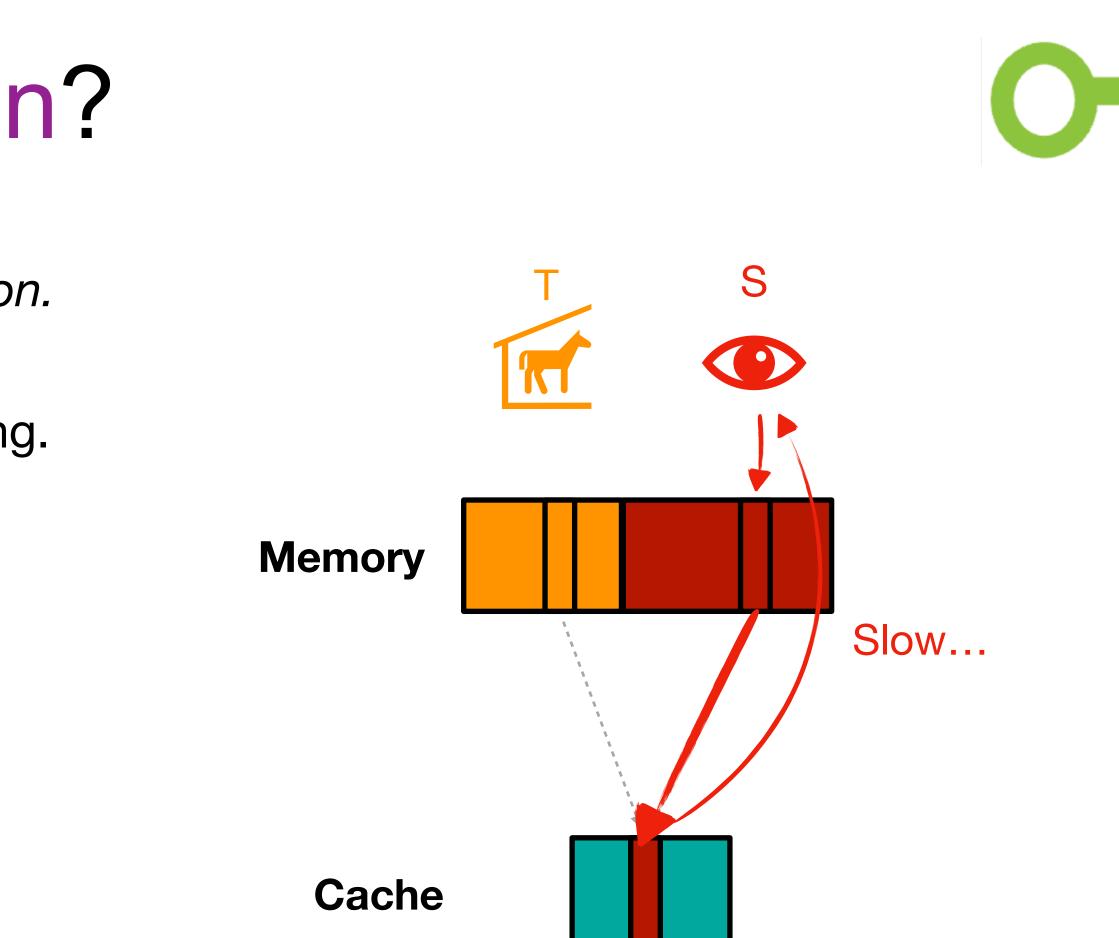




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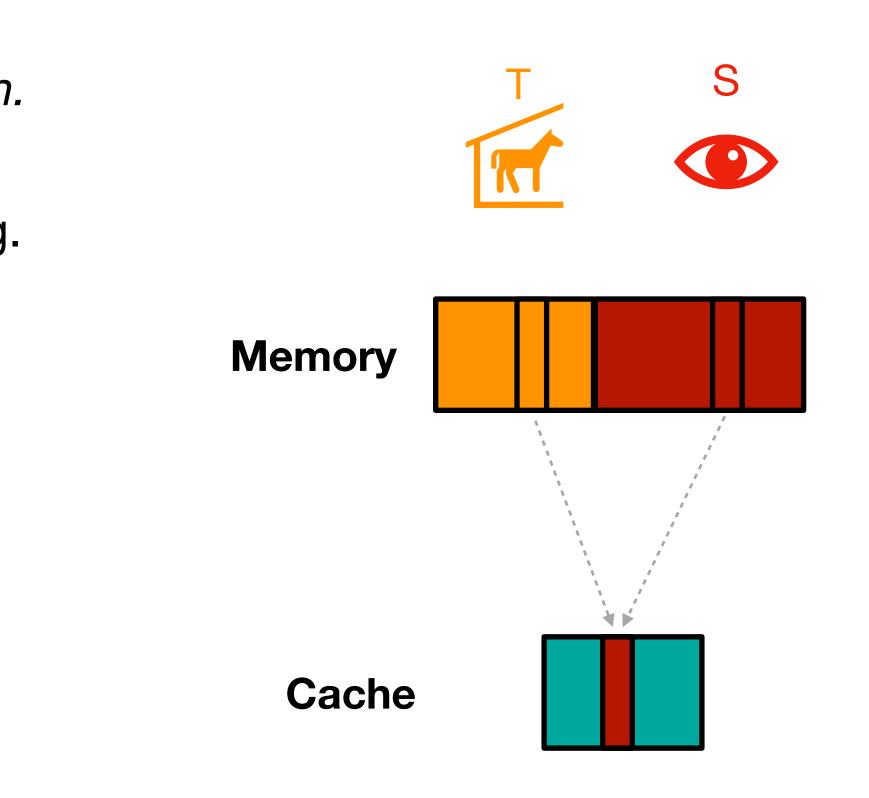




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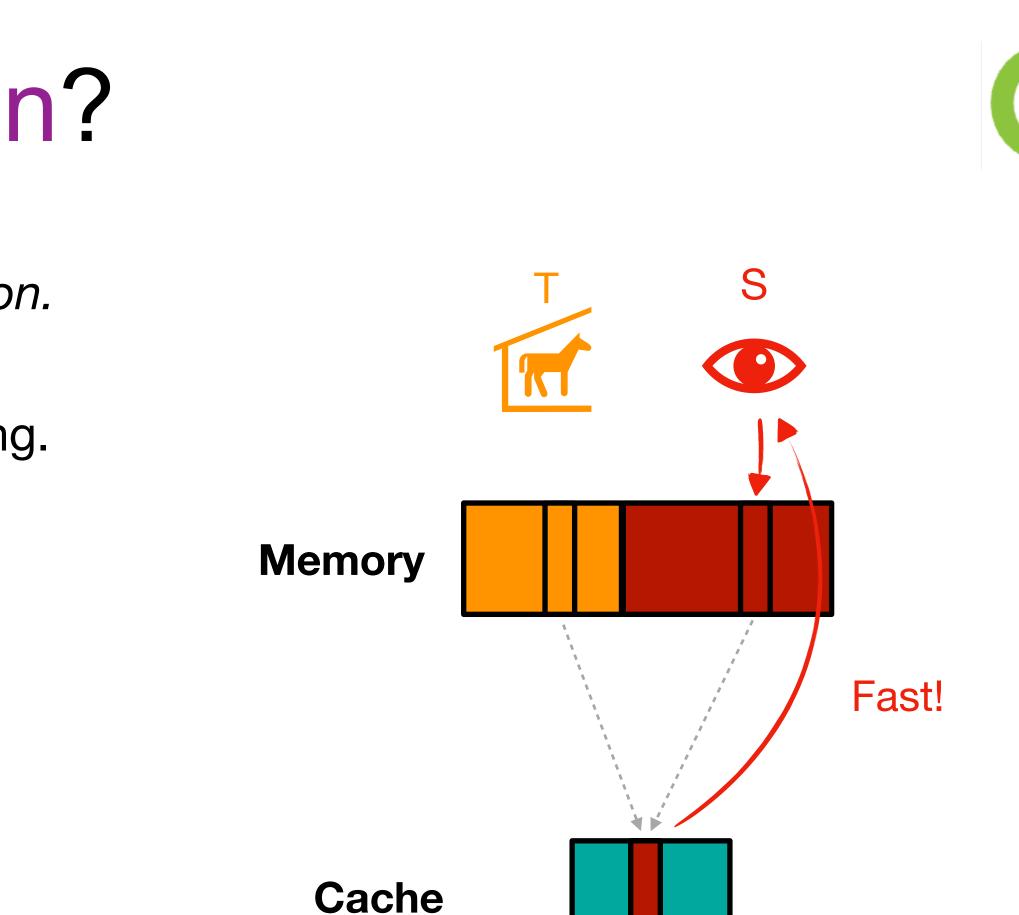








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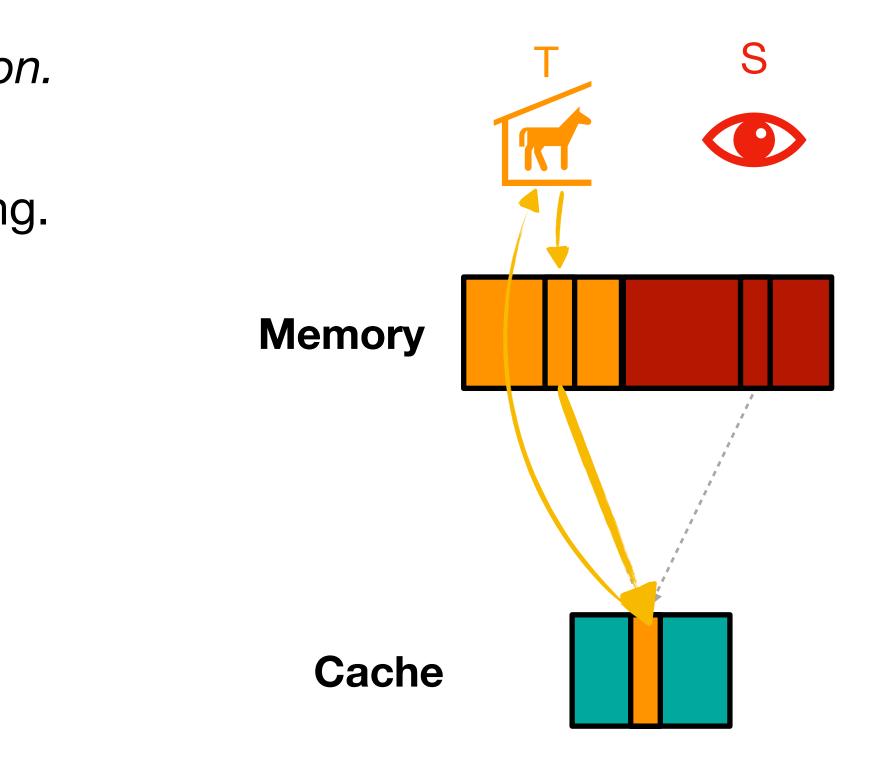






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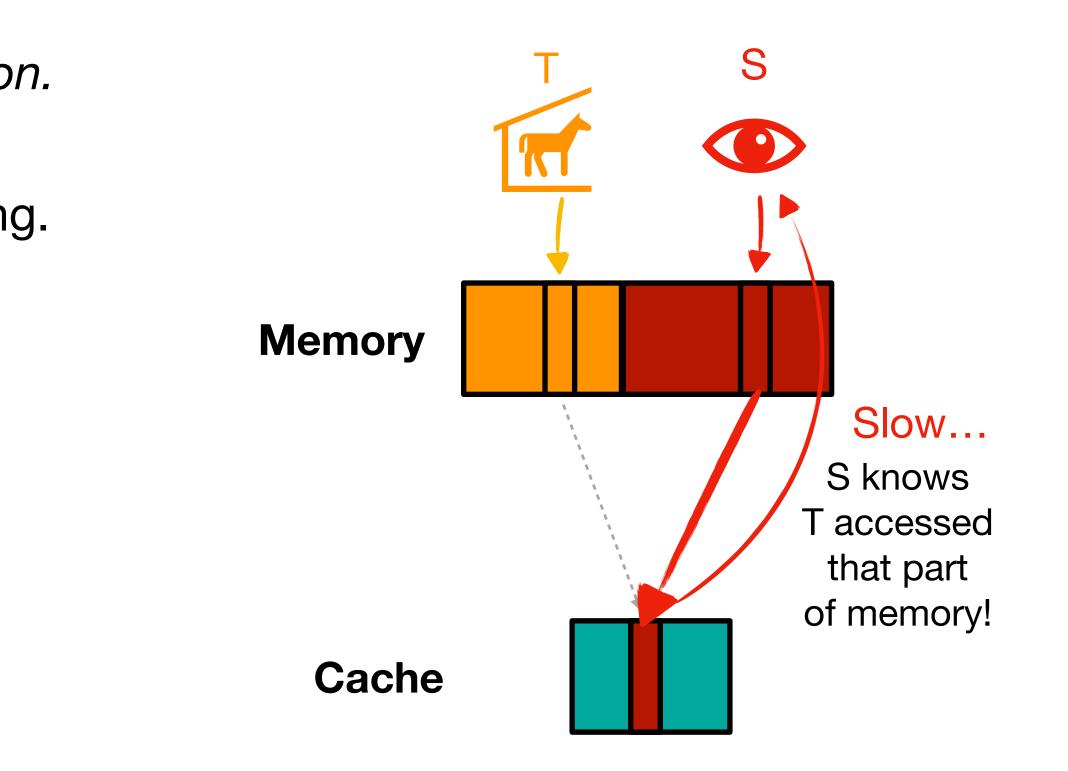


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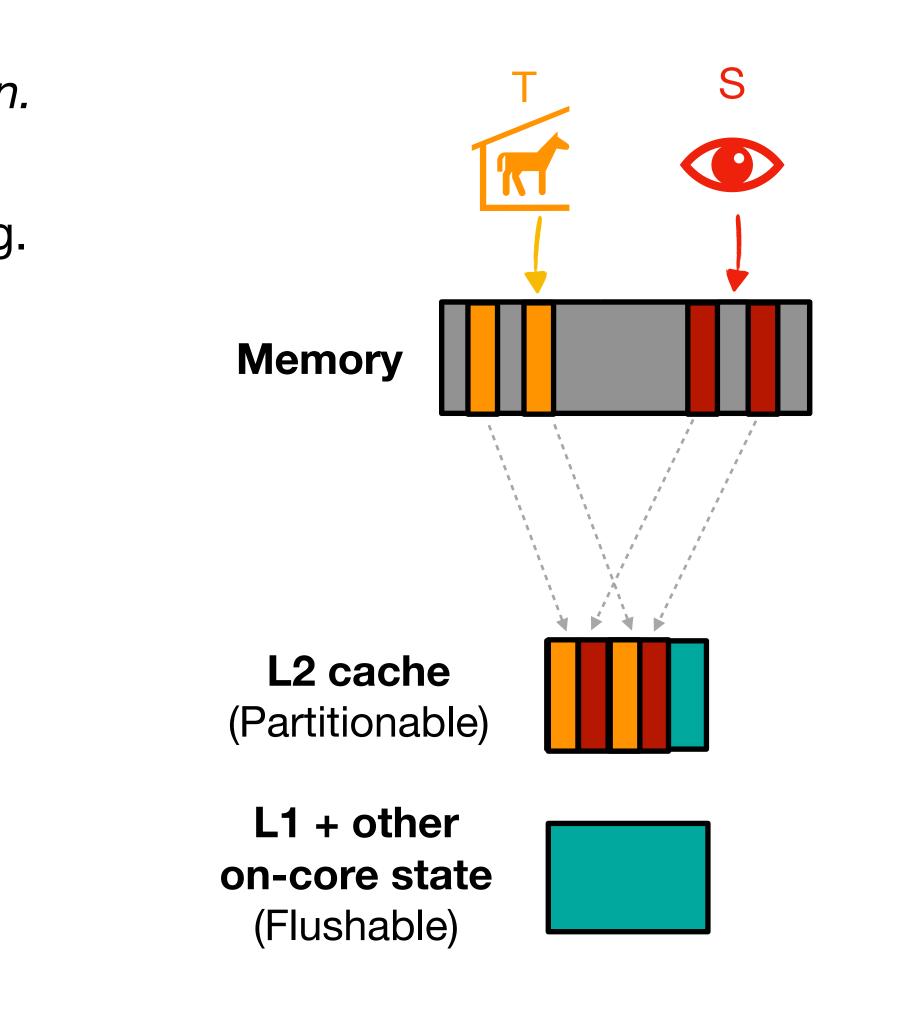






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- To prevent these *timing channels*, OSes can implement *time protection*: See EuroSys: [Ge et al. 2019]
 - *Partition* off-core memory caches





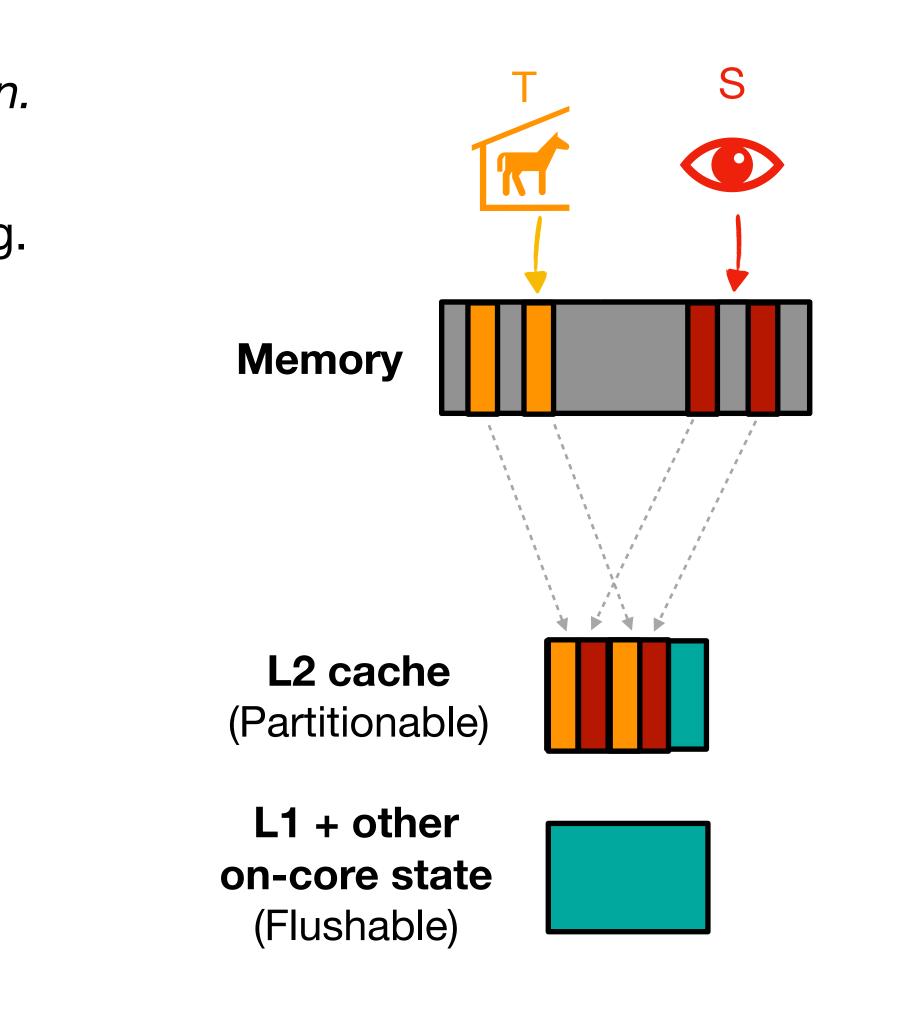


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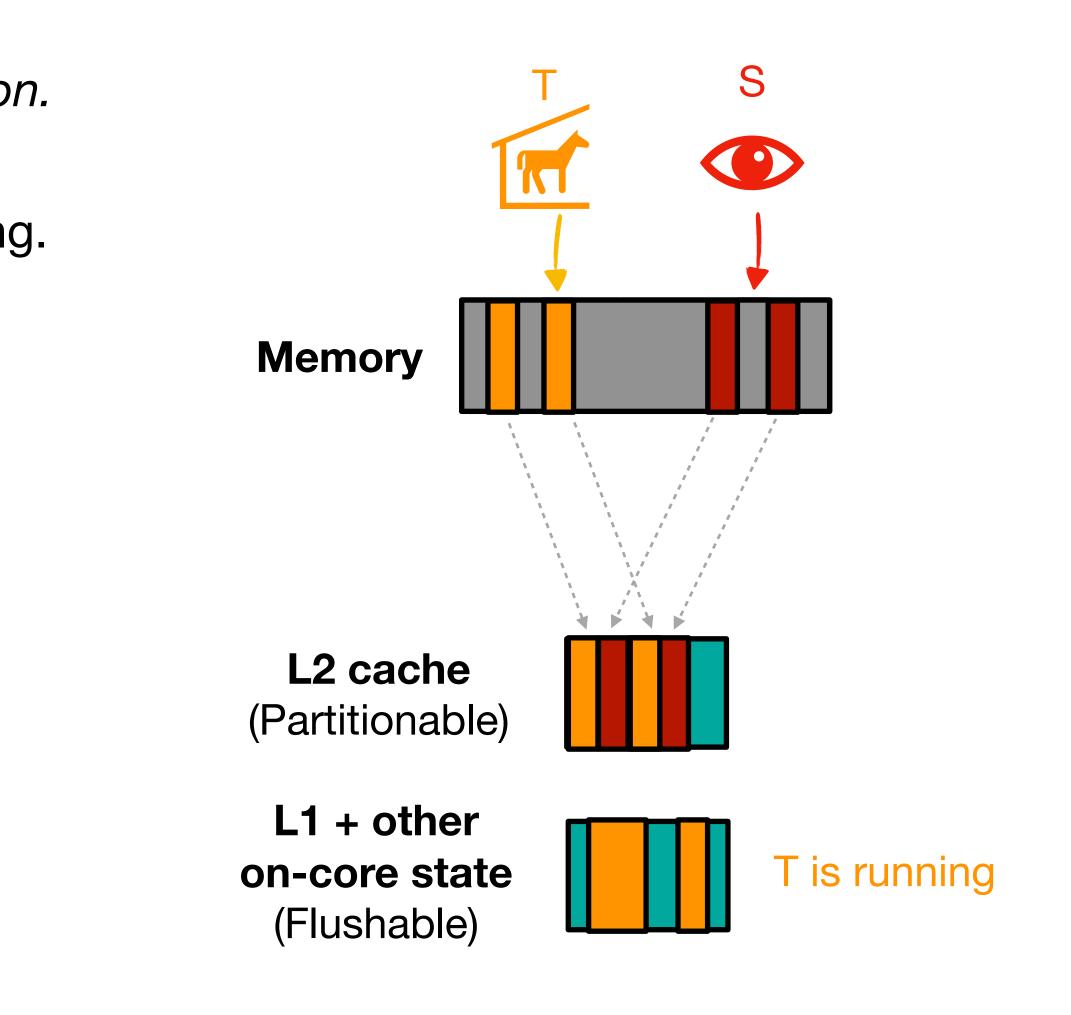


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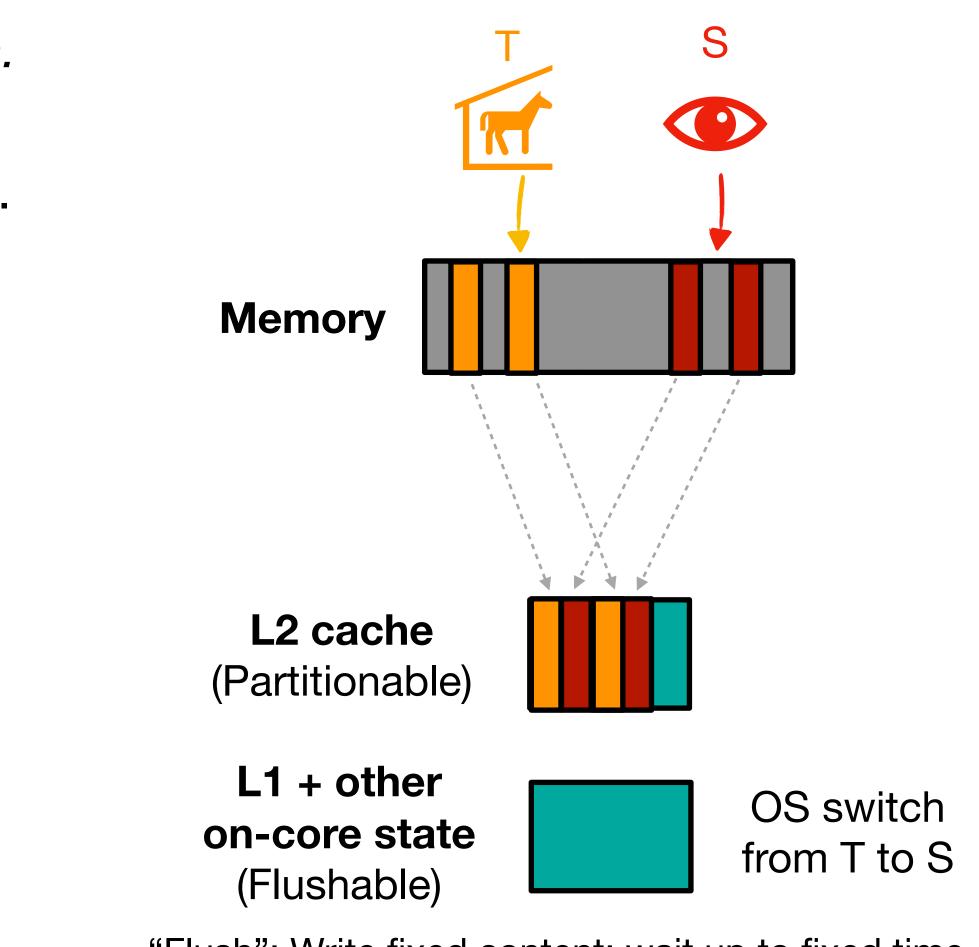






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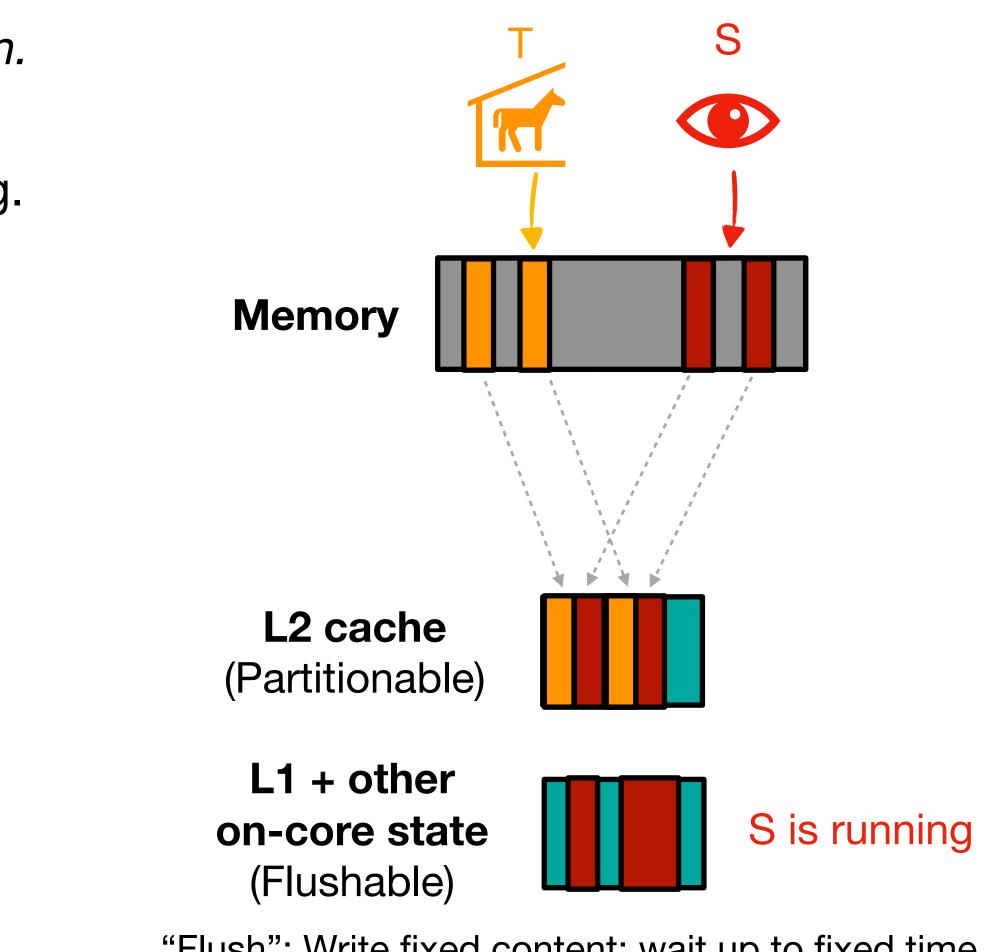
"Flush": Write fixed content; wait up to fixed time.





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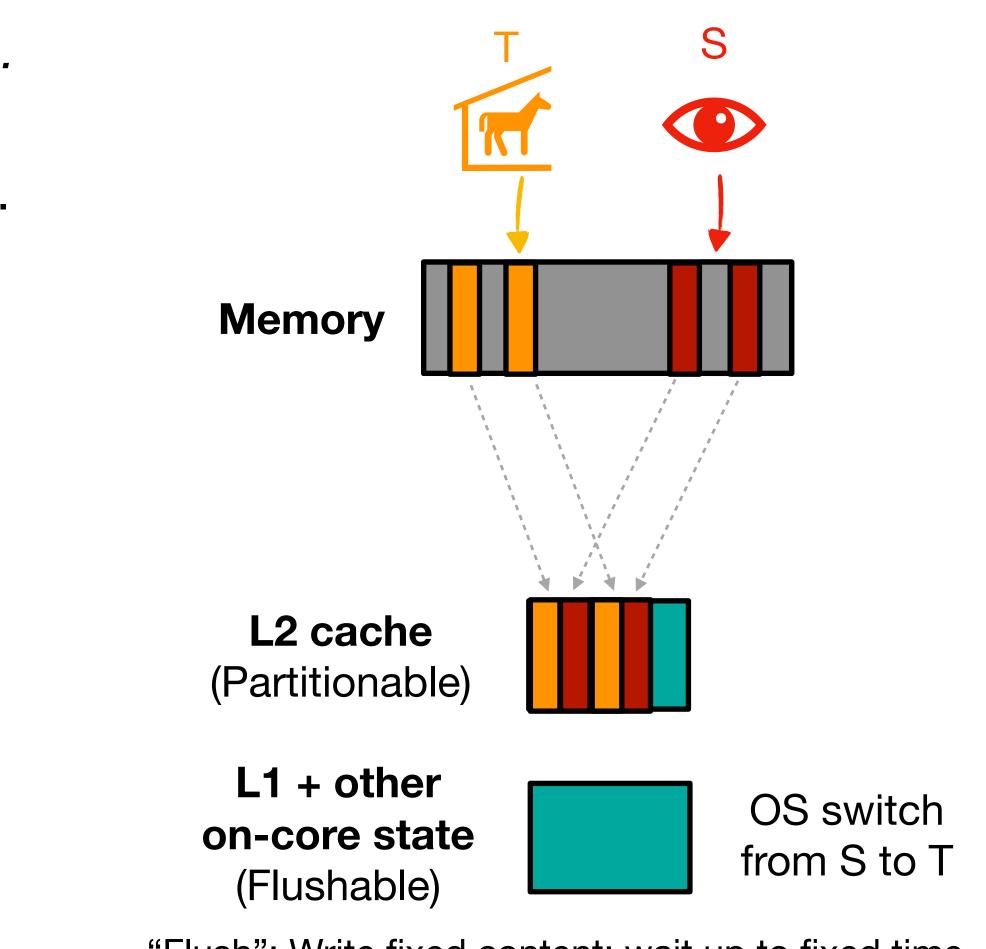
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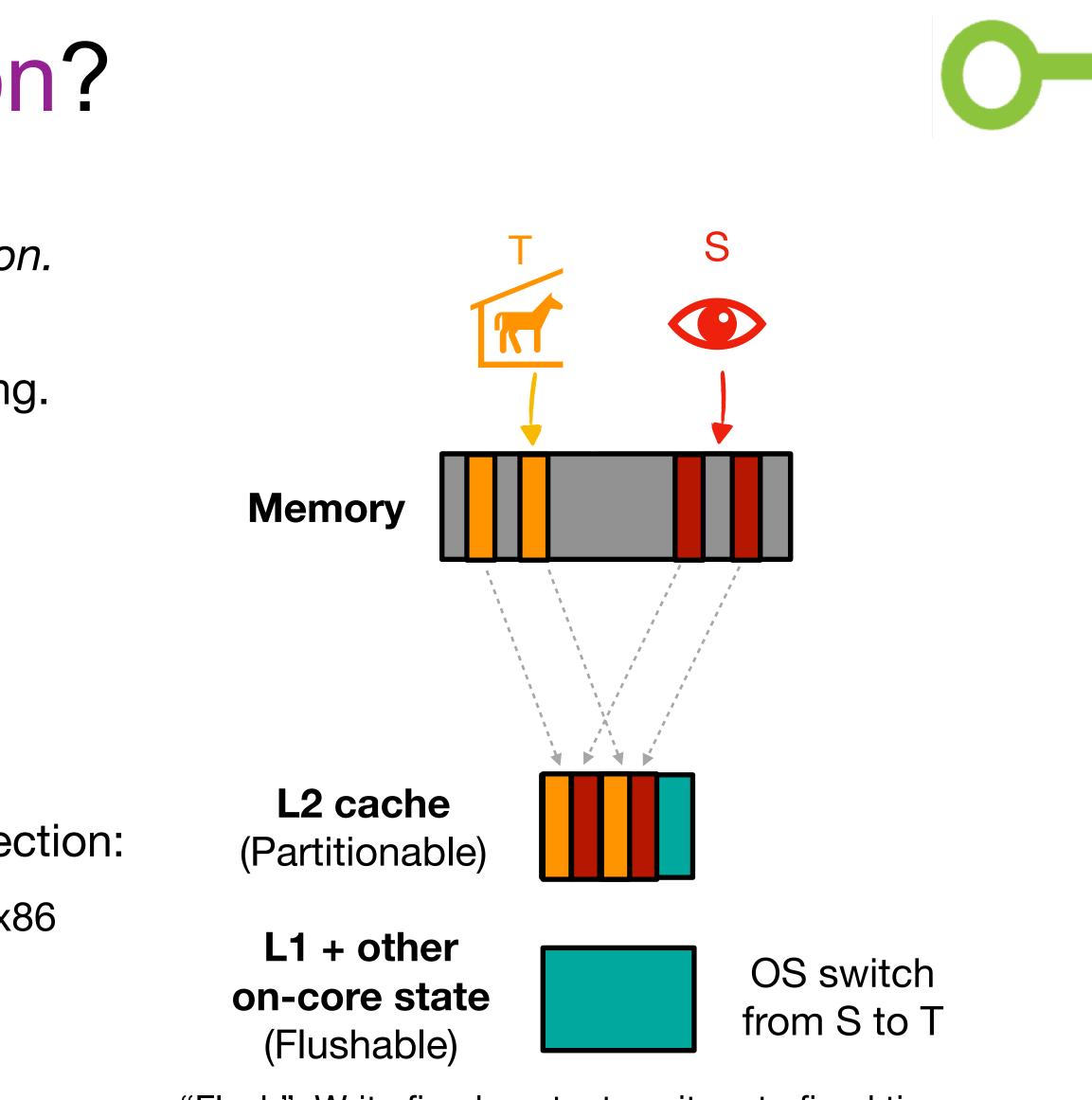


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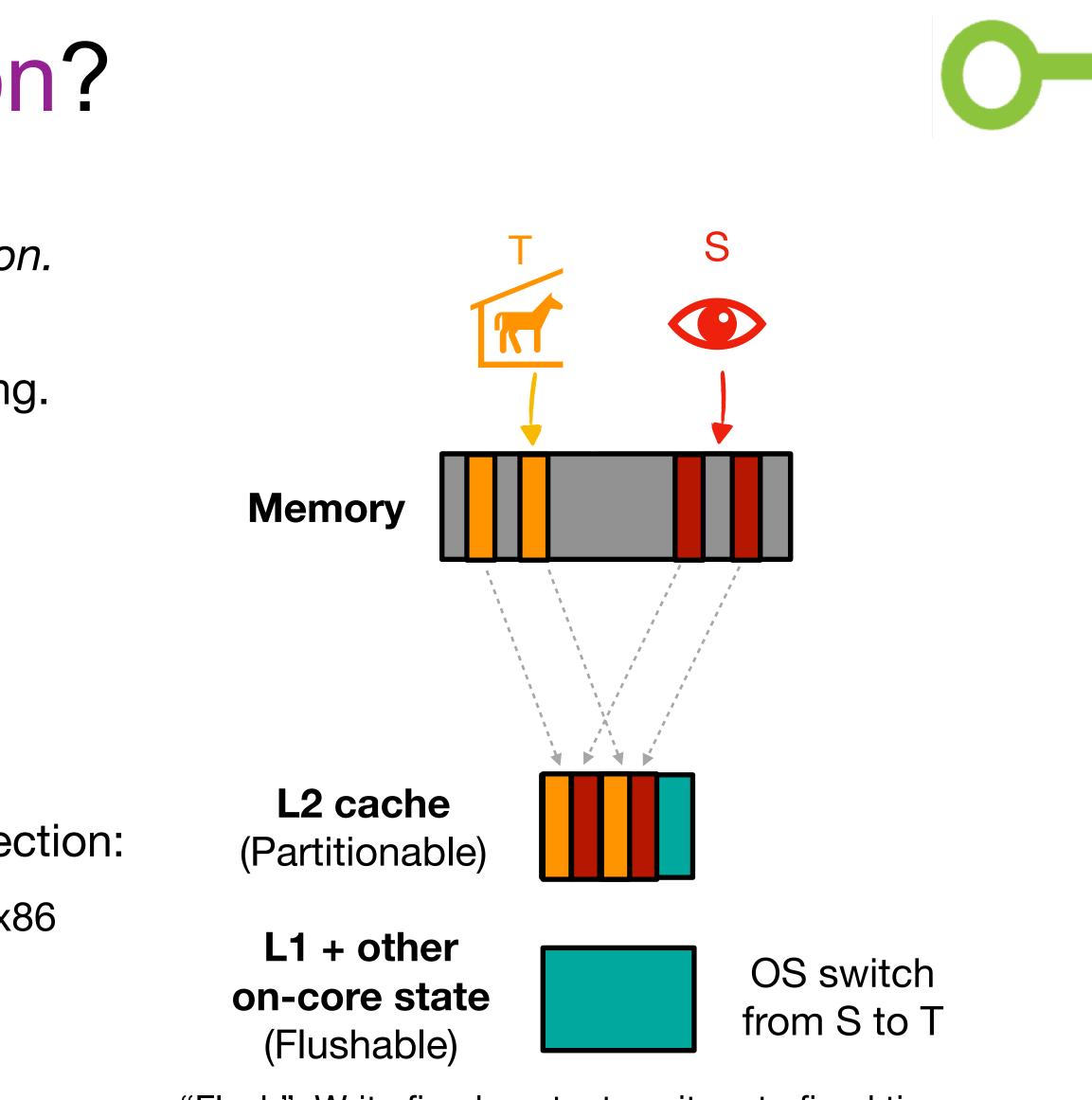


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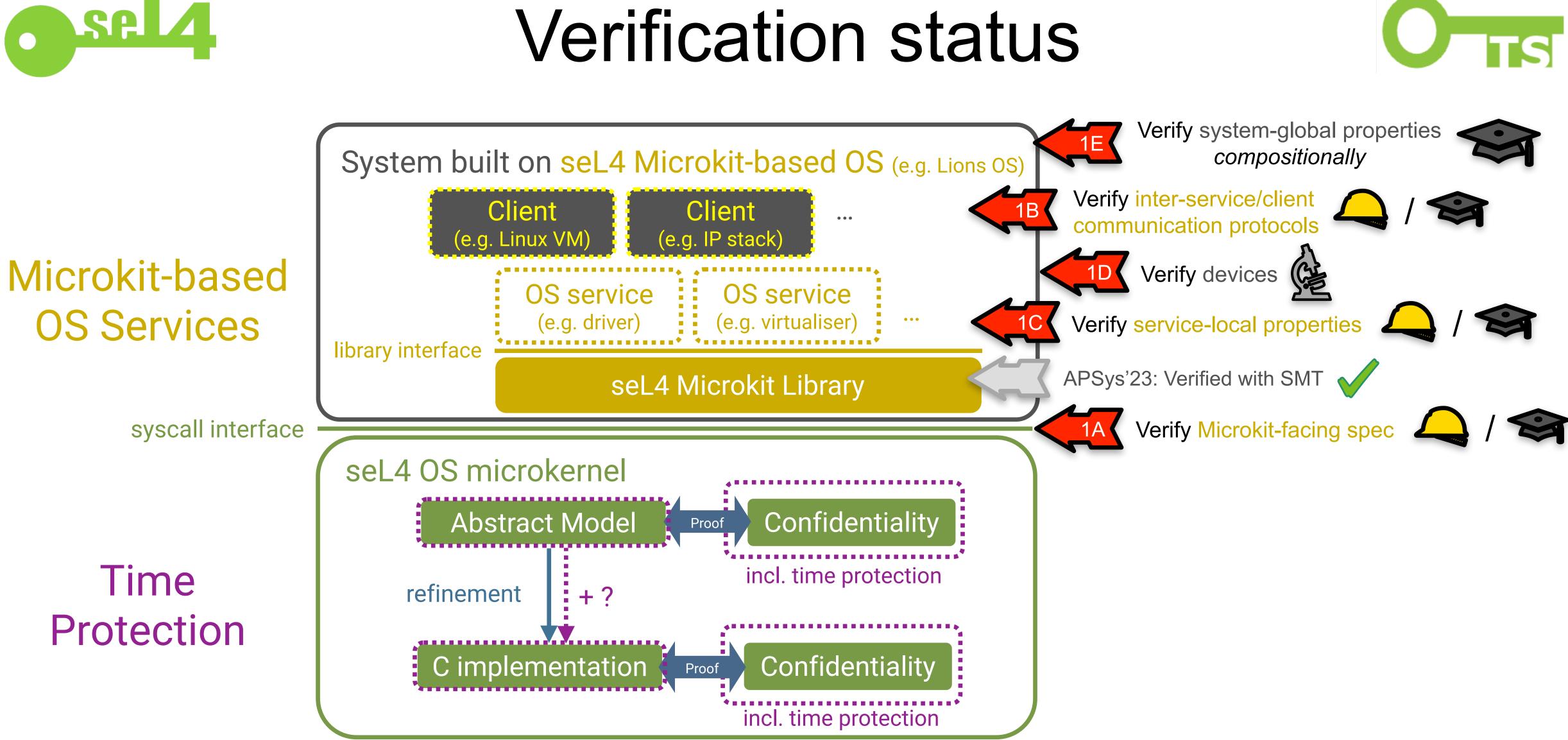


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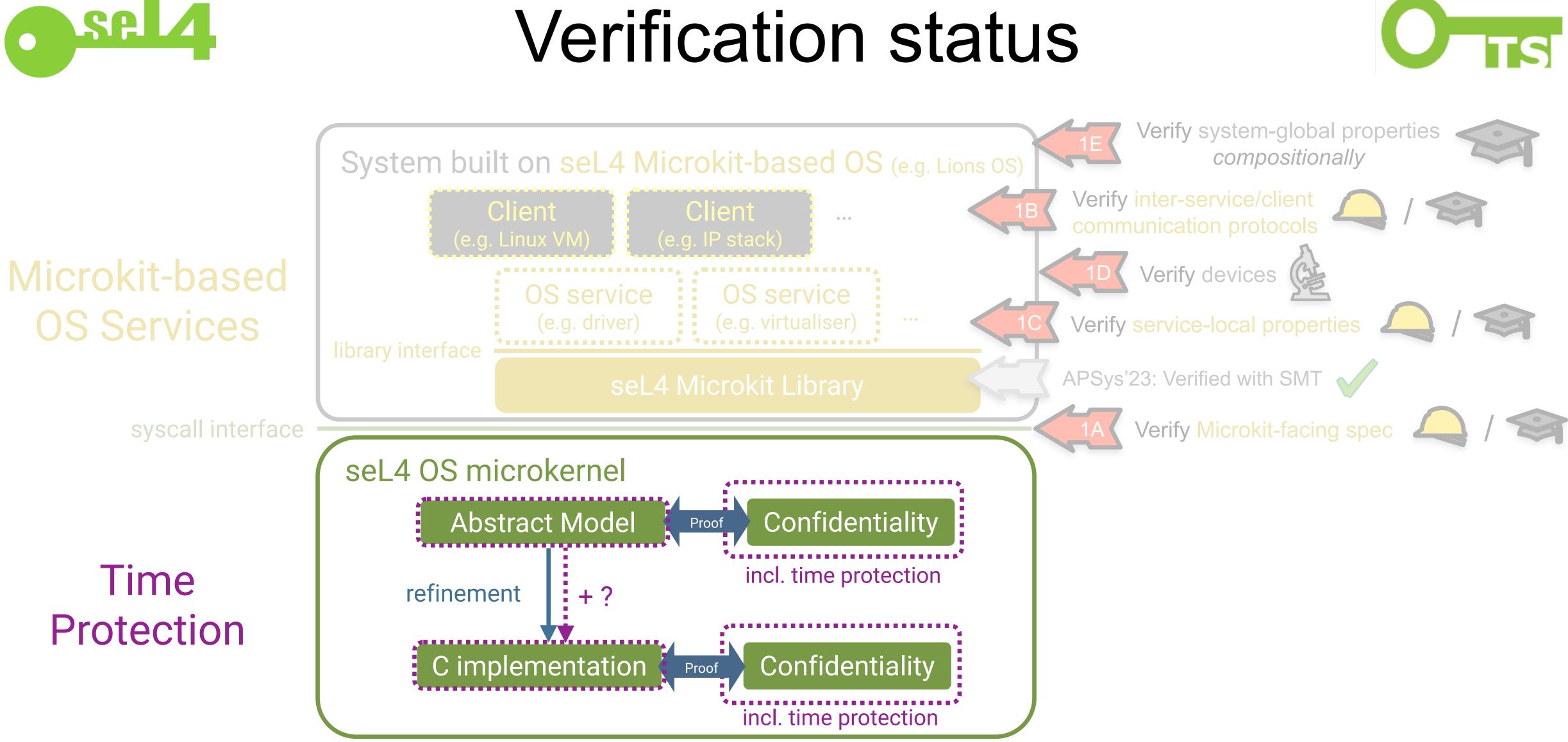










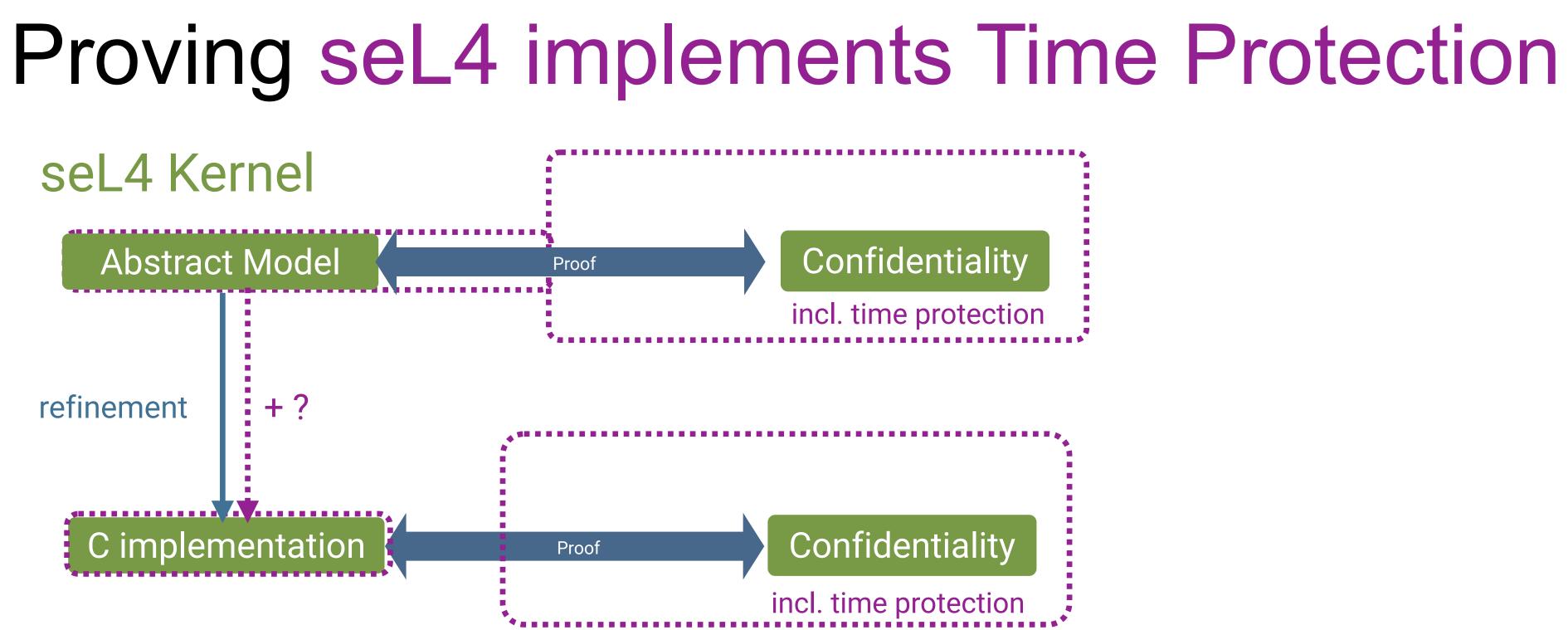




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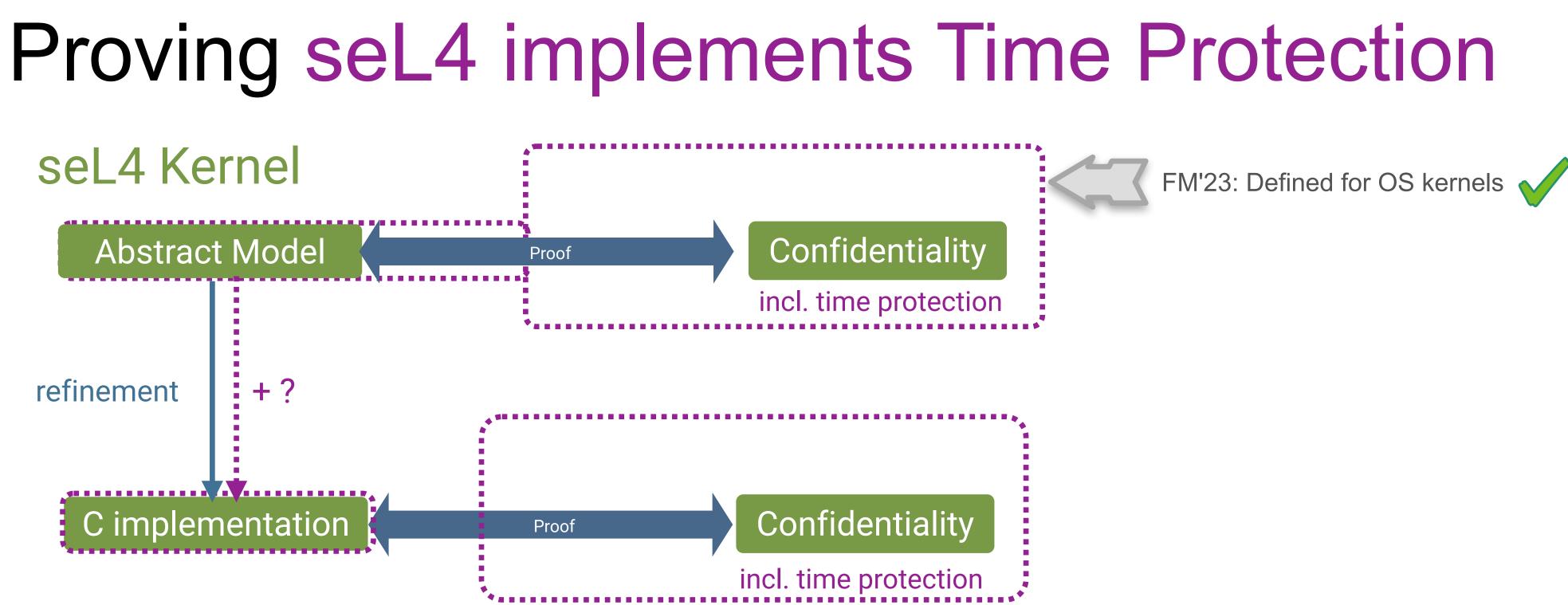


Confidentiality incl. time protection

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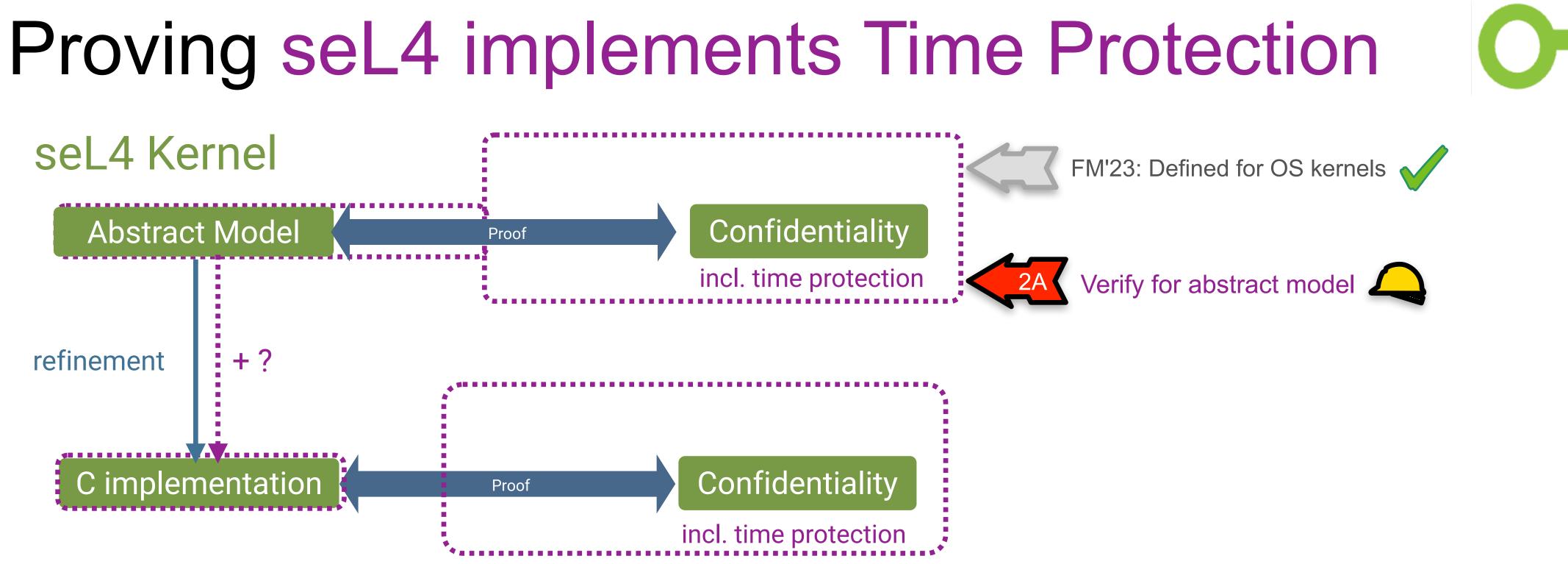








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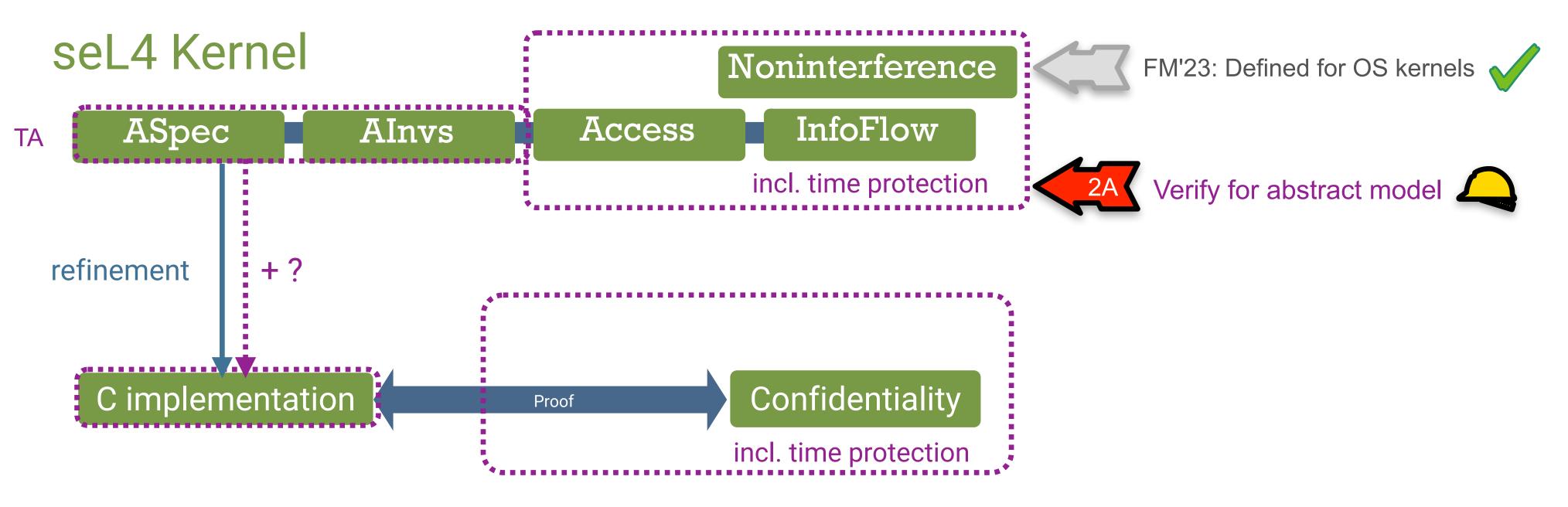




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Proving seL4 implements Time Protection



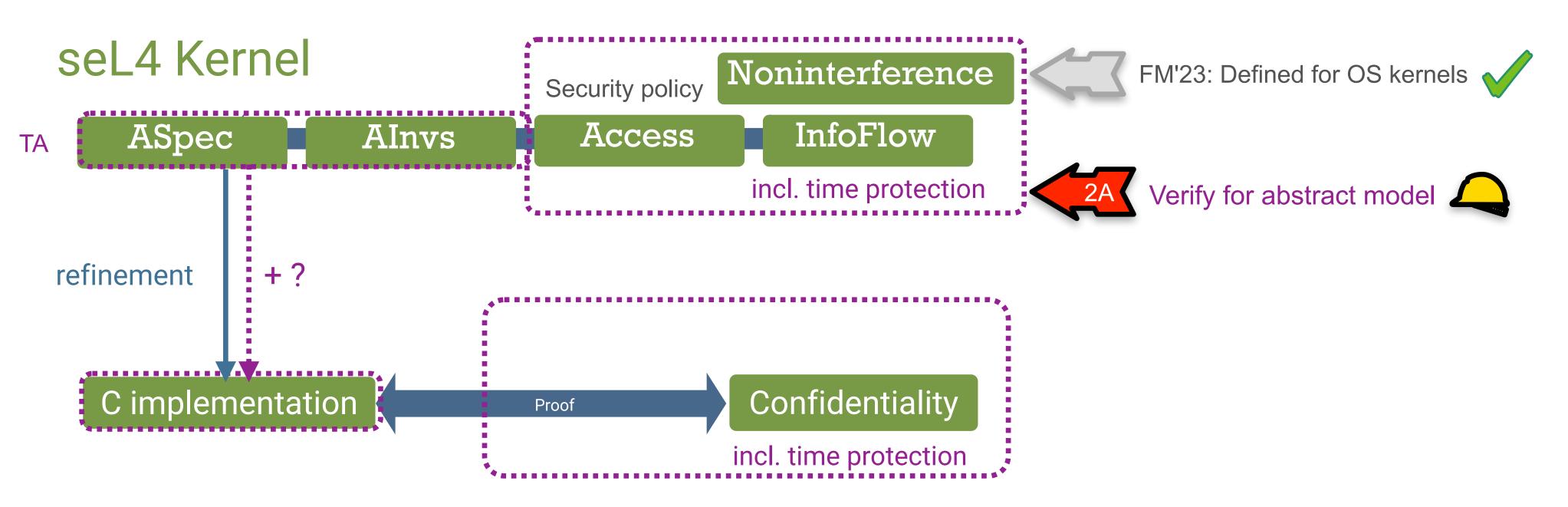
• Abstract model (ASpec) checks touched addresses (TA) set



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Proving seL4 implements Time Protection



- Abstract model (ASpec) checks *touched addresses* (TA) set
- (2A) Key **ASpec** property: TA \subseteq domain's addresses (according to security policy)

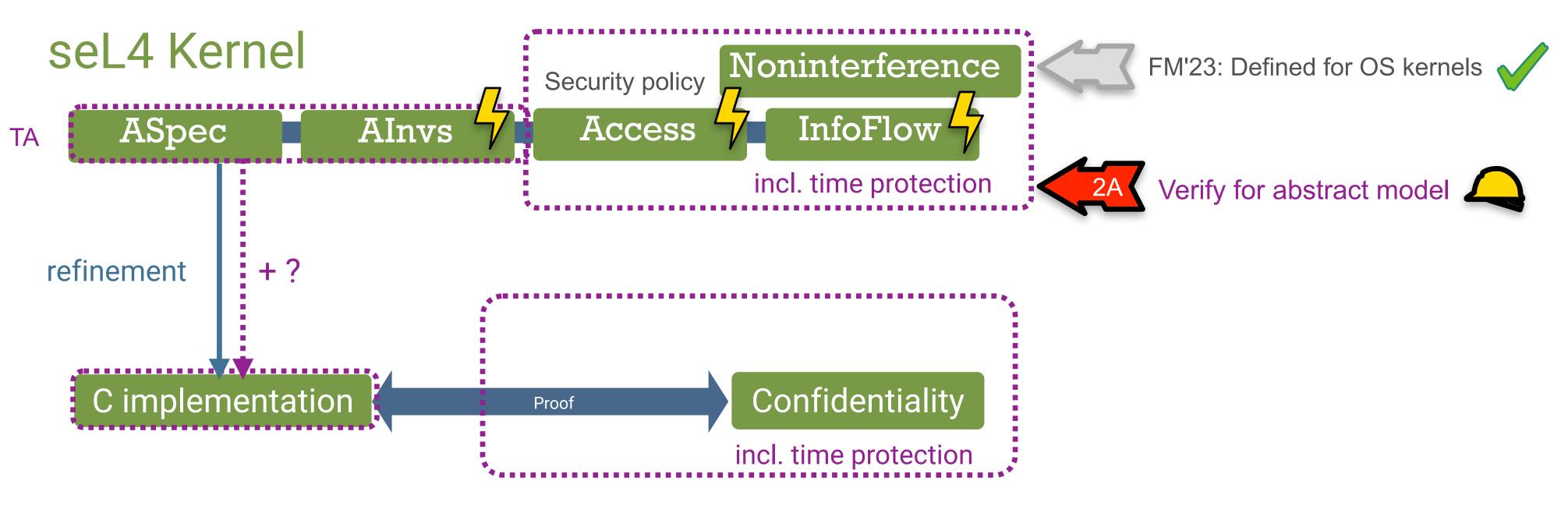




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Proving seL4 implements Time Protection

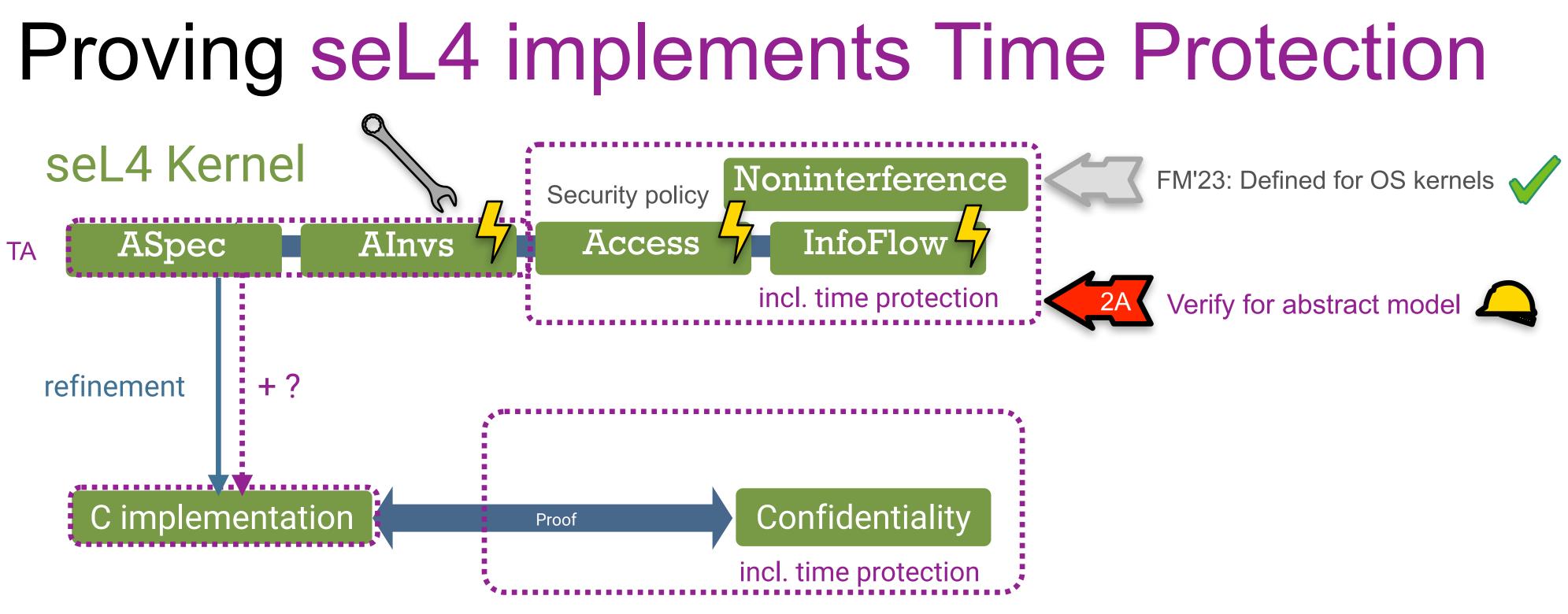


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 - Also: AInvs, Access, InfoFlow need repairs







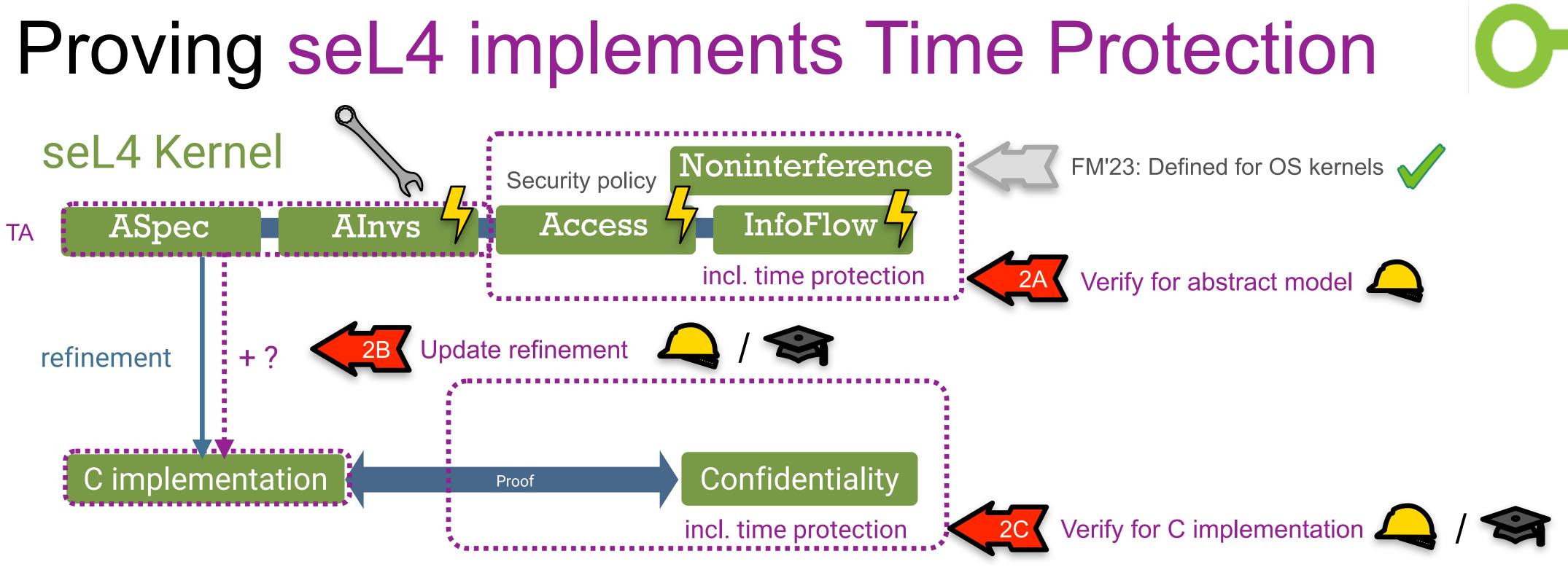


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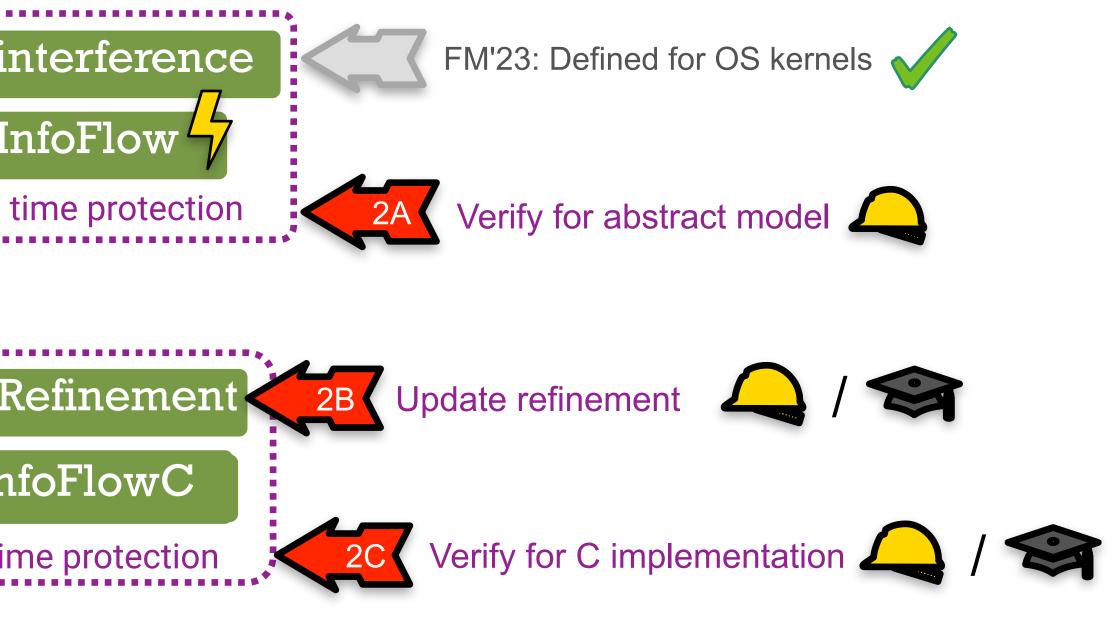






Proving seL4 implements Time Protection seL4 Kernel Noninterference FM'23: Defined for OS kernels Security policy ASpec InfoFlow Access AInvs TA 2A Verify for abstract model incl. time protection refinement 2B ExecSpec TA' refinement +? Noninterference_Refinement 2B Update refinement 2B CSpec InfoFlowC TA" Proof 2C Verify for C implementation incl. time protection

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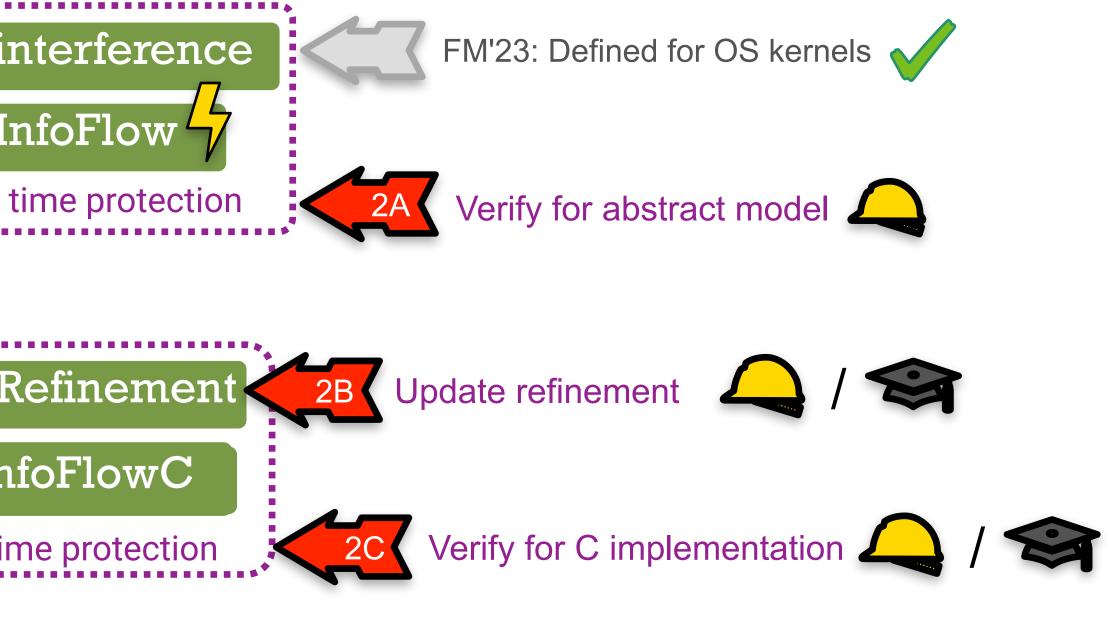






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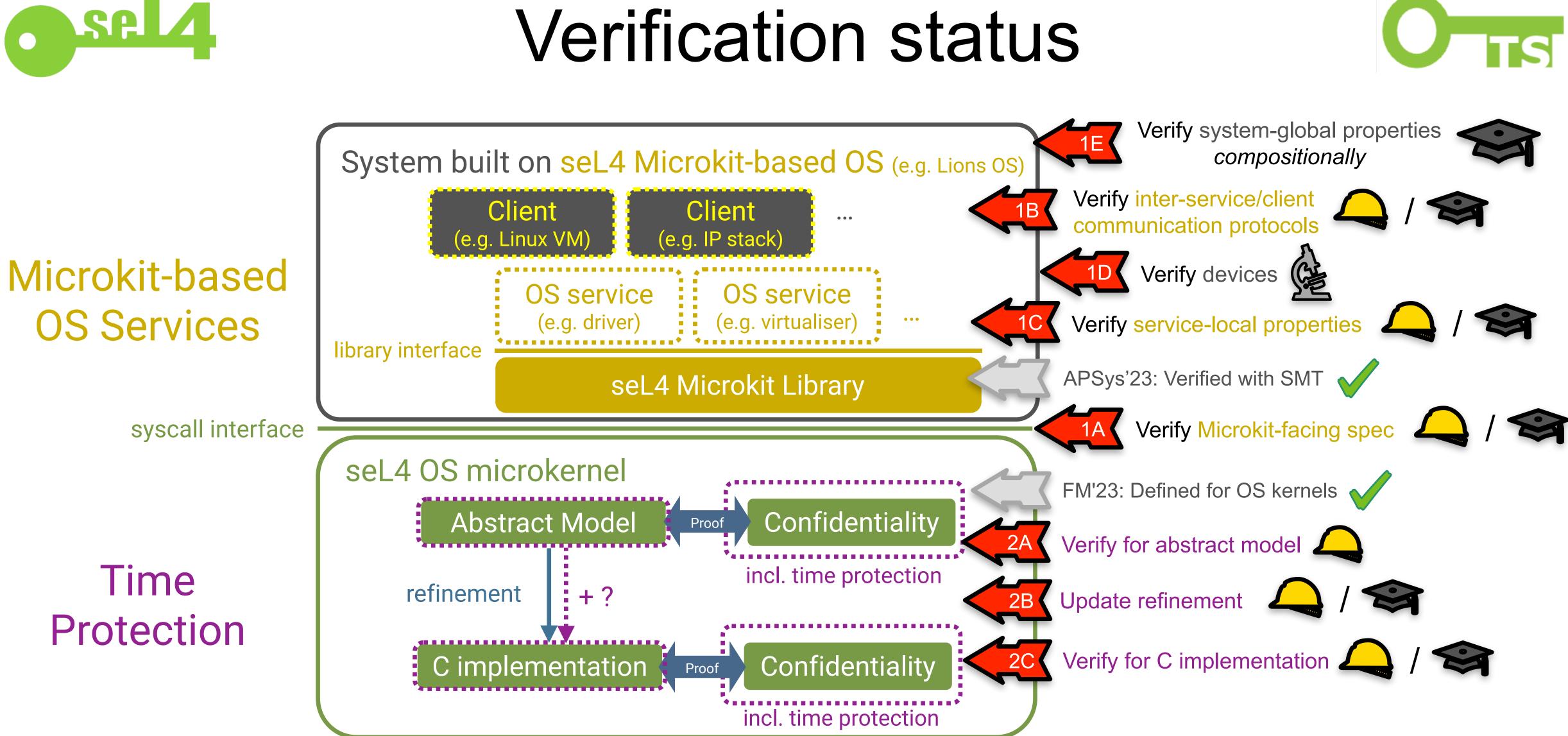
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 - Modulo: Detail on addresses added by refinement to CSpec











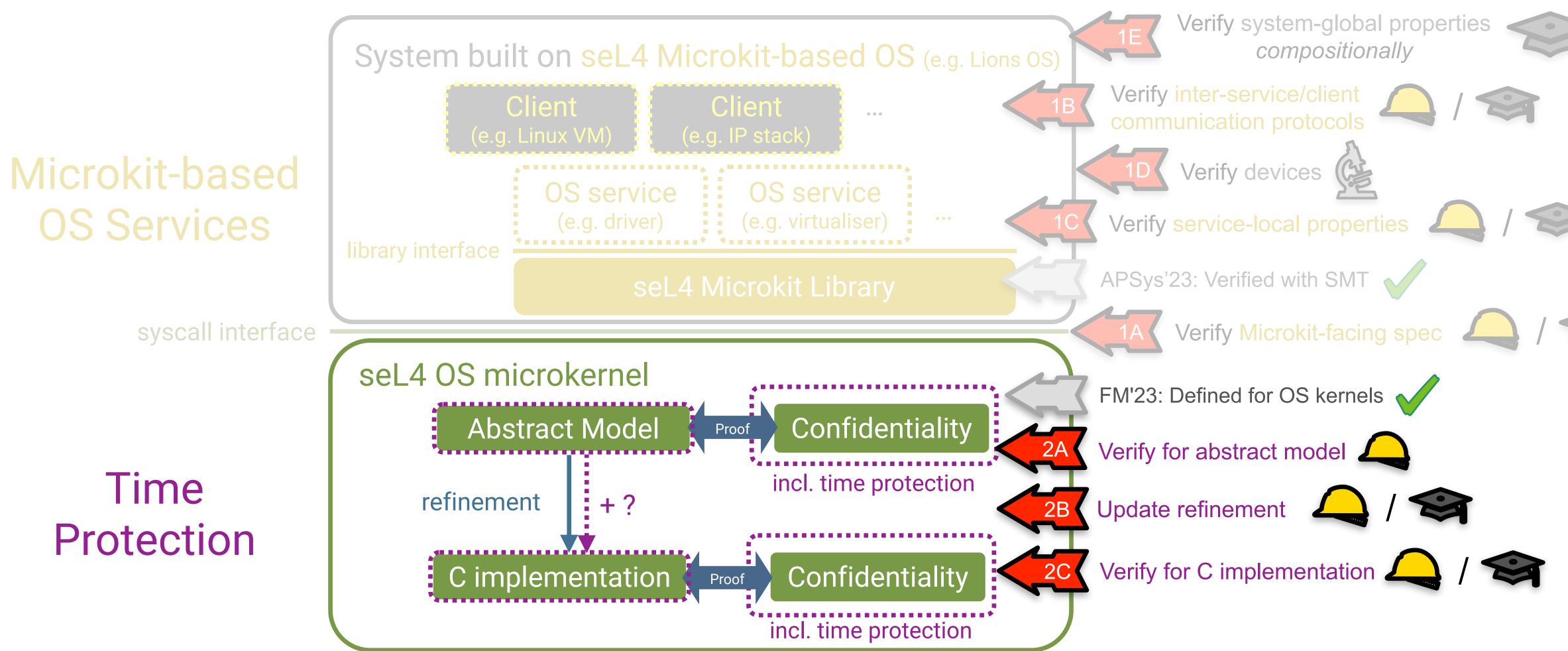








Verification status



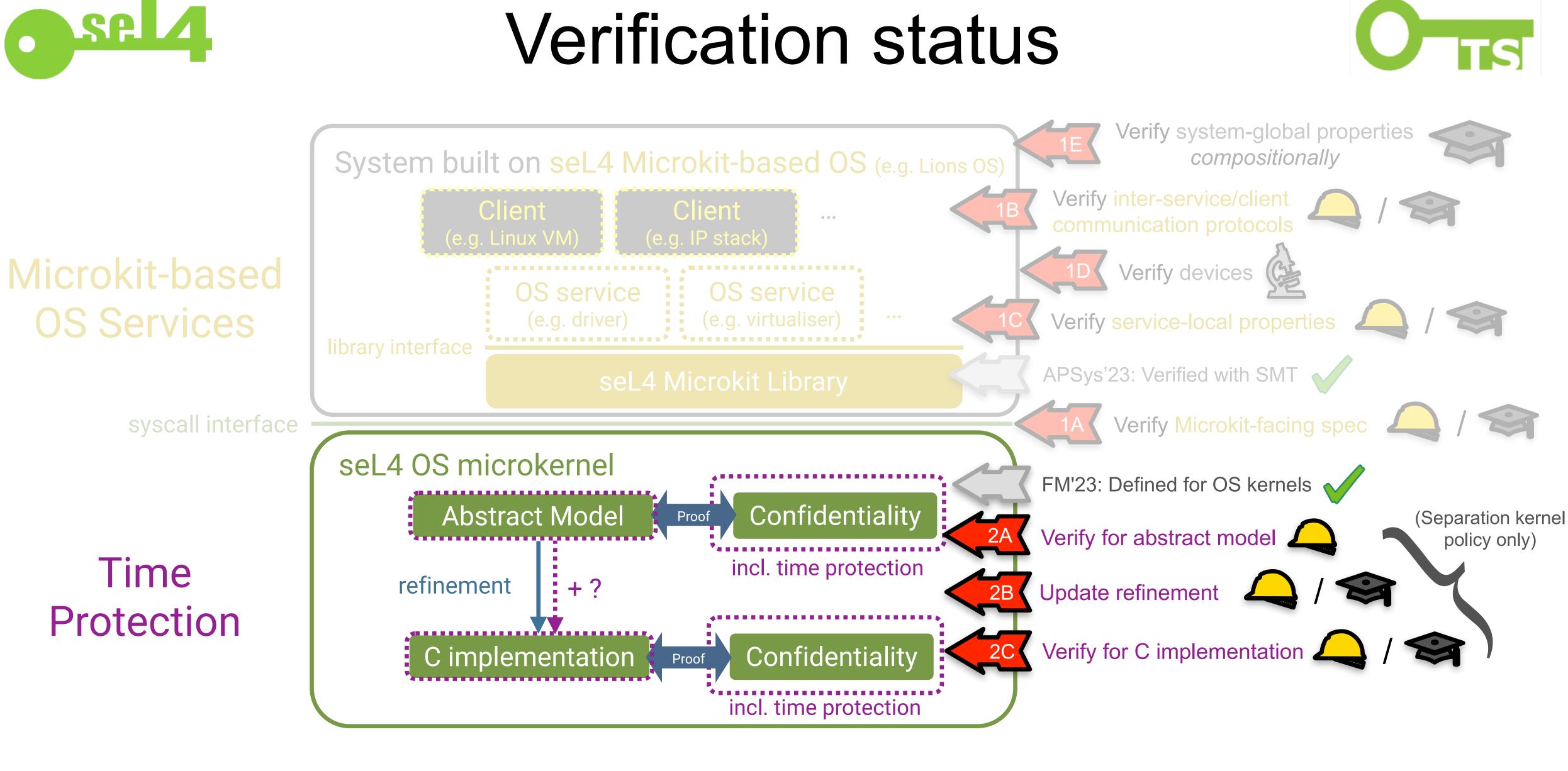








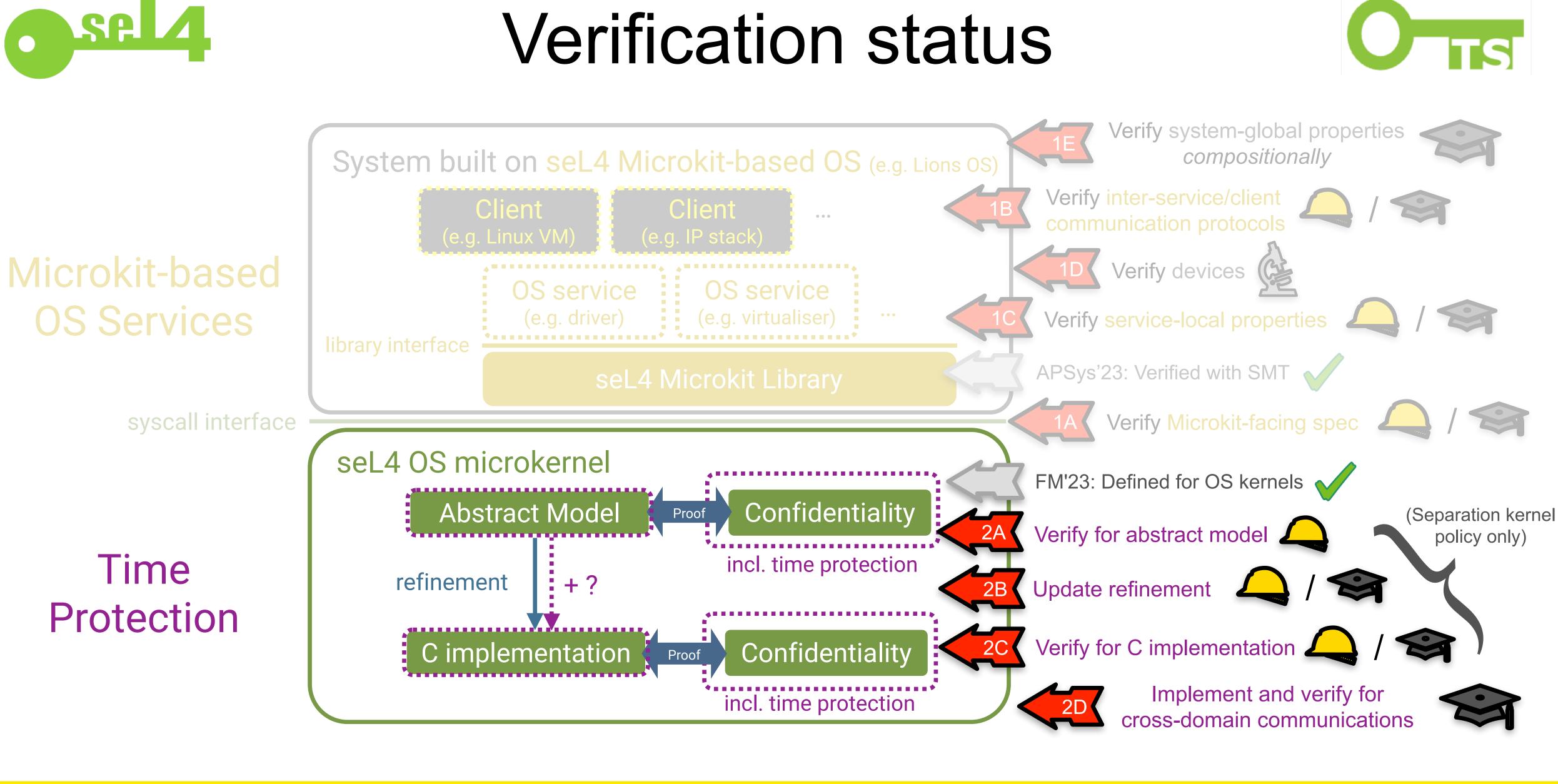








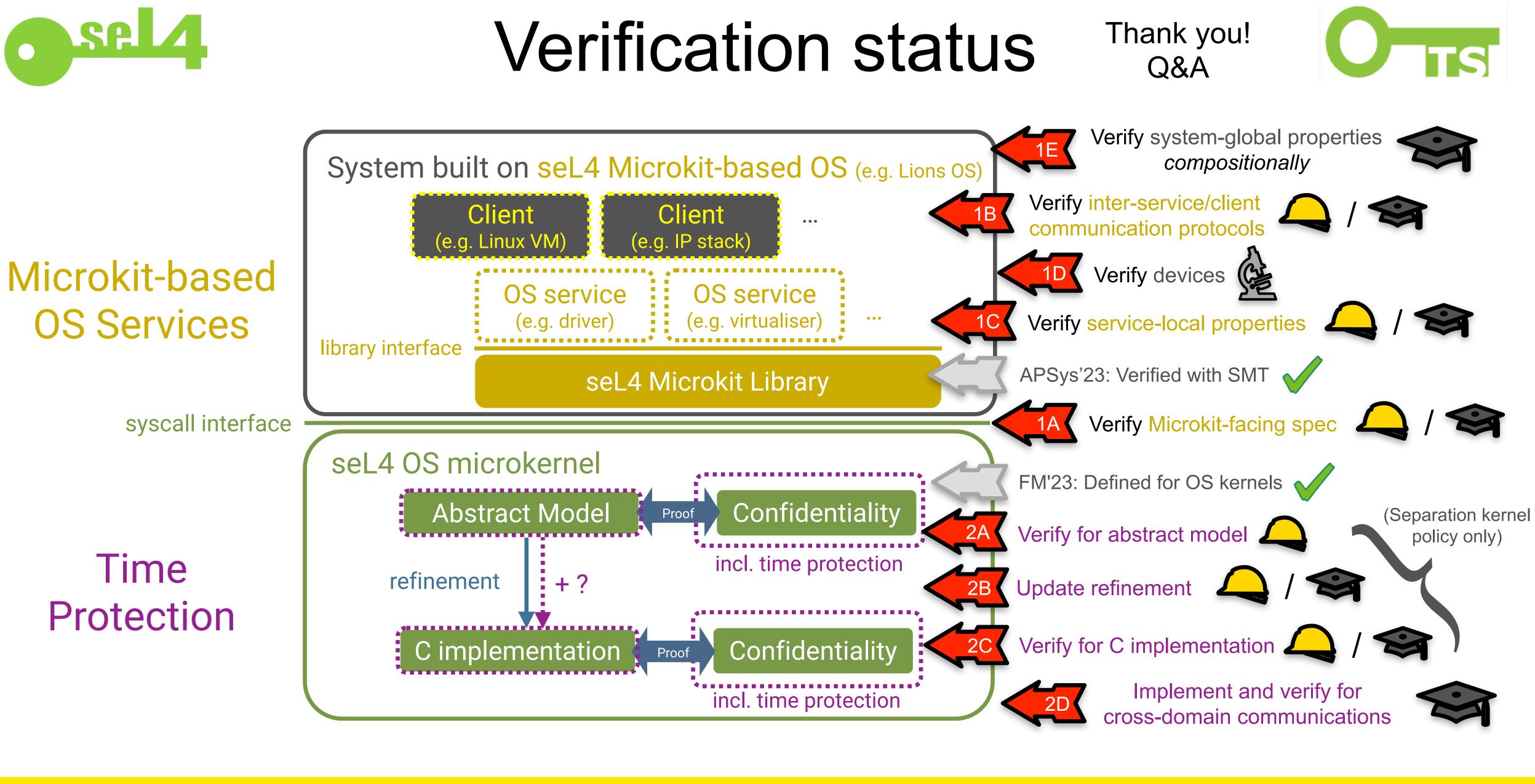




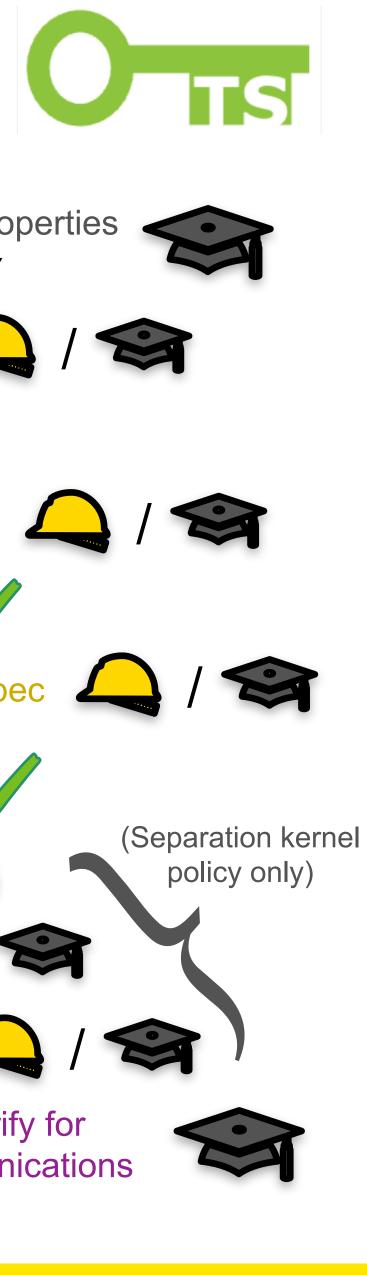
















Trustworthy Systems @ CSE, UNSW Sydney



Verification Status of Time Protection and Microkit-based OS Services, Oct'24



